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STUDIES OF GROWTH-IN DEFECTS AND TRANSPORT PROPERTIES VERSUS GR--ETC(U)
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ANNUAL TECHNICAL REPORT
(For Period: June 11, 1981 to June 10, 1982)

STUDIES OF GROWTH-IN DEFECTS AND TRANSPORT PROPERTIES VS. GROWTH PARAMETERS IN III-V COMPOUND SEMICONDUCTORS

by

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June 1982

This work was performed for the Air Force Office of Scientific Research (AFSC), Bolling Air Force Base, under grant no. AFOSR-81-0187.

TABLE OF CONTENTS

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SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

REPORT DOCUMENTATION PAGE	READ INSTRUCTIONS BEFORE COMPLETING FORM
1. REPORT NUMBER AFOSR-TR- 82-0570	2. GOVT ACCESSION NO. AD-A117 871 / 3. RECIPIENT'S CATALOG NUMBER
4. TITLE (and Subtitle) STUDIES OF GROWTH-IN DEFECTS AND TRANSPORT PRIPERTIES VS. GROWTH PARAMETERS IN III-V COMPOUND SEMICONDUCTORS	5. TYPE OF REPORT & PERIOD COVERED Annual Technical Report June 11, 1981-June 10, 1982
	6. PERFORMING ORG. REPORT NUMBER
7. AUTHOR(s) Sheng S. Li	8. CONTRACT OR GRANT NUMBER(s) AFOSR-81-0187
9. PERFORMING ORGANIZATION NAME AND ADDRESS University of Florida Gainesville, FL 32611	10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS 61102F 2306/B1
11. CONTROLLING OFFICE NAME AND ADDRESS Air Force Office of Scientific Research Bolling Air Force Base, DC 20332	12. REPORT DATE June 10, 1982
	13. NUMBER OF PAGES 87
14. MONITORING AGENCY NAME & ADDRESS(if different from Controlling Office)	15. SECURITY CLASS. (of this report) Unclassified
	15a. DECLASSIFICATION/DOWNGRADING SCHEDULE

16. DISTRIBUTION STATEMENT (of this Report)

Approved for public release; distribution unlimited.

17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)

18. SUPPLEMENTARY NOTES

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

LPE GaAs, VPE GaAs, LEC GaAs; DLTS, C-V, resistivity, Hall effect measurements; grown-in defects, electron trap , EL2 level, trap density, energy level, electron capture cross section, emission rate, electron mobility, annealing effect; carrier density, $Al_{0.3}Ga_{0.7}As$ LPE layer, As_{Ga} and Ga_{As} antisite defects, V_{As} and $(V_{Ga})_2$ defects.

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

The objectives of this research project are: (1) to investigate the grown-in deep level defects vs. growth parameters (e.g., growth temperature, growth rate, Ga/As ratio, and substrate orientations) in GaAs epilayers grown by liquid phase epitaxial (LPE) and vapor phase epitaxial (VPE) techniques, (2) to study the transport properties vs. growth parameters in the LPE and VPE grown GaAs, and (3) to study the effects of combined thermal and injection annealing on the grown-in defects in the VPE GaAs epilayers. Deep-level transient spectroscopy (DLTS) and C-V measurements were performed to study the electron traps in both

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LPE and VPE grown n-type GaAs under various growth conditions (e.g., Ga/As ratios vary from 2/1 to 6/1 for epilayers grown on three different substrates orientations (i.e., <100>, <211A>, and <211B>). Two electron traps with energies of EB4 = E_c-0.71 eV, and EL2 = E_c-0.83 eV were observed in the VPE GaAs samples. For the <211A> (gallium-rich face) oriented samples, the density of EL2 was found to decrease with increasing Ga/As ratio; opposite trend was observed for the <211B> (arsenic-rich face) oriented samples. As for the <100> oriented samples, the density of EL2 level was found to increase or decrease with increasing Ga/As depending on the type of defects formed during the growth of these epilayers. In the GaAs epilayers grown by the infinite solution melt liquid phase epitaxial (LPE) technique, two growth temperatures (700 and 800°C) and two cooling rates (1°C/min. and 0.4°C/min.) were used. Results of the DLTS and C-V measurements on these samples showed that only one electron trap with energy of E_c-0.71 eV (i.e., EB4 level) was observed in samples grown at 700 and 800°C with 1°C/min. cooling rate; none was observed in samples with 0.4°C/min. cooling rate. Electron mobility at 77 K was found lower for samples with 1°C/min. cooling rate than those with 0.4°C/min. cooling rate. This result shows that faster cooling rate will result in higher trap density and lower electron mobility than those with slower cooling rate. Study of the deep level defects in p-type GaAs grown by liquid encapsulated Czochralski (LEC) technique was also carried out. A hole trapwas observed in the samples with energy equal to E_v+0.080 eV, and electron traps with energies of E_c-0.12 to E_c-0.18 eV were also observed in these samples. The 80 meV hole trap is due to double acceptor Ga_{As} antisite defect, and the EL2 trap is attributed to the As_{Ga} antisite defect, as confirmed by other recent works. In addition to the study of grown-in defects in the VPE, LPE, and LEC GaAs, studies of the grown-in defects in $Al_{0.3}Ga_{0.7}As$ LPE layers have also been made in this work, and the results are described in the appendix.

I. INTRODUCTION

The present understanding of deep-level defects in GaAs and other III-V compound semiconductors is presented by a substantial number of publications in the literature [1-9], but still leaves much to be desired after two decades of study. Speculations on the physical nature of native defects and complexes are still very tentative and uncertain. It is not even possible to assign with any assurance a simple gallium vacancy (V_{Ga}) or arsenic vacancy (V_{As}) related defect to a particular energy level observed in gallium arsenide.

In one aspect understanding has been improved. GaAs specimens grown by various techniques such as LPE, VPE, MOCVD, MBE, and LEC, are now recognized as likely to have different properties in terms of energy levels within the bandgap due to differences in defect energy levels and trace impurities or impurity complexes. For examples GaAs grown by liquid-phase epitaxy (LPE) technique from a gallium melt is expected to be low in gallium vacancy defects and possibly high in arsenic vacancies. LPE GaAs usually contains hole traps with energy levels of E_v+0.40 eV (A-center) and E_v+0.71 eV (B-center), while VPE GaAs layers grown in arsenic-rich conditions always contain an electron trap with energy of E_c-0.83 eV (EL2 level). The reason for observing these levels in the LPE and VPE GaAs is still not clear. Also depending on the construction of the system and the care with which it has been prepared and cleaned, the VPE GaAs epilayers may contain additional levels other than the EL2 level. Deep-level defects play an important role in influencing the material properties and device performance. The deep-level defects may (1) reduce carrier mobility due to increase in ionized impurity scattering, (2) change carrier density from shallow impurities, (3) reduce device speed due to trapping

effect, (4) degrade device performance via nonradiative recombination and trapping mechanisms.

The goal of this research program is to conduct a systematic study of the grown-in deep level defects and transport properties in GaAs specimen grown by the VPE, LPE, and LEC techniques under various growth conditions. To achieve this research goal, four LPE GaAs samples, twelve VPE GaAs specimens and three LEC GaAs samples were prepared for this study. For the LPE GaAs samples, two growth temperatures (i.e., 700°C and 800°C) and two temperature drop rates (1°C/min. and 0.4°C/min.) were employed. For the VPE GaAs specimens, the GaAs epilayers were grown on the <100>, <211A>, and <211B> oriented semi-insulating C -doped GaAs substrates. The gas phase stoichiometry was controlled by varying the Ga/As ratios from, 2/1, 3/1, 4/1, 5/1, to 6/1. Deep-level defects were characterized by the DLTS and C-V measurements. Carrier density and carrier mobility were determined by the resistivity and Hall effect measurements. DLTS and C-V measurements were also made on several p-GaAs specimens grown by the liquid encapsulated Czochralski (LEC)technique. The energy level for each electron and hole trap as well as capture cross section were deduced from the DLTS and C-V data for the VPE, LPE, and LEC GaAs samples studied. Correlations between the grown-in defect parameters and the growth parameters were obtained for the VPE and LPE GaAs samples. Study of the low temperature thermal annealing and recombination enhanced annealing effects on the grown-in deep level defects has also been made for the VPE GaAs specimens. Details of our technical findings will be described in this report. Section 2.0 reviews the possible native defects and impurity complexes in GaAs. Section 3.0 discusses the method of calculating the defect concentration as a function of temperature and arsenic pressure for several point defects in GaAs.

The growth of GaAs epilayers by the VPE and LPE techniques and the structure of GaAs Schottky barrier diodes are described in section 4.0. Section 5.0 depicts the resistivity and Hall effect measurements in the GaAs samples. The results of TSCAP and C-V measurements are described in section 6.0. Section 7.0 presents the results of the DLTS measurements. The thermal and injection annealing mechanisms and the results for the VPE GaAs are described in section 8.0. The effects of combined thermal and recombination-enhanced annealing on the EB4 and EL2 electron traps are discussed in this section. Section 9.0 gives the summary and conclusions derived from this work. Lists of interactions with individuals from government and industrial labs, publications, personnel involved in this project are given respectively in section 10.0, 11.0, and 12.0. References are given in section 13.0, and Appendix is given in section 14.0 which contains paper describing the results of our study of grown-in defects in the $Al_{0.3}Ga_{0.7}As$ and GaAs epilayers grown by LPE technique.

II. REVIEW OF POSSIBLE NATIVE DEFECTS AND COMPLEXES IN GALLIUM ARSENIDE

The number of possible native defects in GaAs is large as may be seen in table 1. None of these native defects has been identified with any confidence. This is due to the fact that experiments for studying such defects tend to be too uncontrollable. In addition to the defects shown in table 1, other types of defects such as impurities, complexes of impurity atoms with native defects may also be expected in GaAs.

In this report, we will focuss our discussions only on a few native defects listed in table 1, which are believed to be related to the electron traps observed in our LPE and VPE GaAs specimens studied here. Defects due to impurities or impurity complexes will not be discussed in this report.

Defects can be represented by symbols, atoms being represented by their normal chemical symbol, vacancies by V. Subscripts indicate the lattice site, characterized by the atom normally occupying that lattice site. Thus, V_A is a vacancy at an A site. Interstitial site are indicated by a subscript, i, A_i being A atom at an interstitial site. For examples, in table 1, V_{Ga} denotes the gallium vacancy; Ga_i represents the gallium interstitial site defect. In addition to these simple vacancy defects, grown-in defects as a sample cools down might be expected to cluster to form neutral complexes such as $V_{Ga}As_{Ga}V_{Ga}$. Another type of defect, namely, the antisite defect, must also be considered. The anticite defects, such as As_{Ga}^{+2} and Ga_{As}^{-2}, and the bound pairs of these antisite defects, $As_{Ga}Ga_{As}$, which constitute a neutral defect, are believed to be important native defects in GaAs specimen. Theoretical calculations of the

formation energy for the $As_{Ga}Ga_{As}$ defect showed that the value should be around 0.70 to 0.72 eV for GaAs, in good agreement with experimental observation. It is interesting to note that formation energies for the antisite defects in III-V compounds are normally less than the formation energies of vacancies or interstitials; this implies that antisite defects are present in compound semiconductors in substantial concentrations. Fig. 2.1 illustrates some of the possible native defects and complexes in GaAs materials.

Table 1.1. Possible Native Defects in Gallium Arsenide

1. <u>One component defects</u>:
   a. Vacancy: V_{Ga}, V_{As}
   b. Interstitial: Ga_i, As_i

2. <u>Two component defects</u>:
   a. Divacancy: $V_{Ga}V_{Ga}$, $V_{As}V_{As}$, $V_{Ga}V_{As}$.
   b. Antisite: Ga_{As}, As_{Ga}
   c. Di-interstitial: Ga_iAs_i
   d. Vacancy-interstitial complex: $V_{Ga}Ga_i$, $V_{Ga}As_i$, $V_{As}Ga_i$, $V_{As}As_i$

3. <u>Three component defects</u>:
   a. Antisite-vacancy complex: $As_{Ga}V_{Ga}$, $As_{Ga}V_{As}$, $Ga_{As}V_{Ga}$, $Ga_{As}V_{As}$
   b. Trivacancy: $V_{Ga}V_{As}V_{Ga}$, $V_{As}V_{Ga}V_{As}$.

4. <u>Four component defects</u>:
   a. Antisite-divacancy complex: $V_{Ga}As_{Ga}V_{Ga}$, $V_{As}Ga_{As}V_{As}$
   b. Diantisite: $Ga_{As}As_{Ga}$

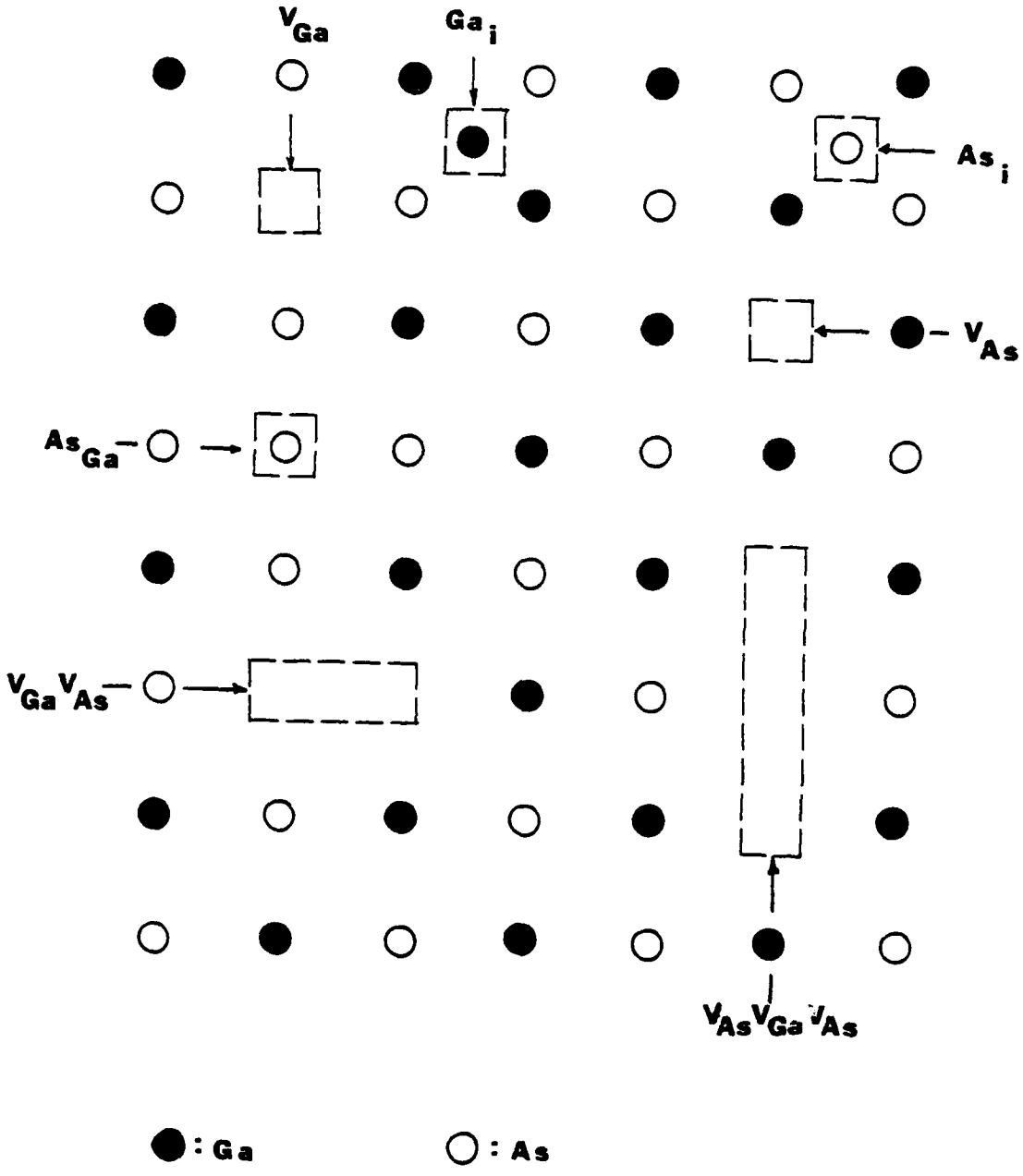

Fig. 2.1 Possible native defects and complexes in gallium arsenide

III. THEORETICAL CONSIDERATIONS OF POINT DEFECTS AND NONSTOICHIOMETRY IN GALLIUM ARSENIDE

The most likely defects expected to be present in GaAs during the crystal growth are point defects. The compositional range for the intermetallic zincblende structure phase in GaAs extends from 49.998 to 50.009 at % As [10]. This corresponds to concentration of 4×10^{18} As vacancies per cm^3 and 2×10^{19} Ga vacancies per cm^3, respectively [11], assuming that non-stoichiometry results in vacancies only. Using lattice parameter measurements, Potts and Pearson [12] observed concentrations of the order of 10^{19} cm^{-3}, which they identified as As monovacancies. By means of measurements of damping by internal friction, Chakraerty and Dreyfus [13] observed a similar concentration of defects, which they tentatively identified as Ga divacancy. In EPR measurements, Goldstein and Almeleh [14] observed concentration greater than 10^{19} cm^{-3} of some resonance centre which they considered to be some combination of point defects. The standard methods of chemical thermodynamics are used to derive expressions for the equilibrium concentrations, as a function of temperature and arsenic pressure. We consider here only the following types of point defects: arsenic monovacancies V_{As}^{x}, gallium monovacancies V_{Ga}^{x}, gallium divacancies $(V_{Ga})_2^{x}$ and appropriately charged versions of these three. Charged states is represented by the different subscriptions [15]. The subscripts "," represents negative charge, "x" represents neutral states and "." indicates positive charge. Thus $(Ga)_2'$ represents a negatively charged Ga divacancy.

The method of analysis may be outlined as follows [16]: One can write down a reaction equation for the formation of each type of defects in the solid and for the formation of electrons and holes. There is a further reaction equation

representing the transfer of atoms between the gas and solid phases. For each of these reactions there is a mass action which applies at equilibrium. The mass action reaction can be written in terms of concentrations and Boltzmann statistics used for the electrons. To these mass action conditions, one adds the condition of electroneutrality and the resulting set of equations can be solved for the defect concentrations in terms of the partial pressure of the arsenic. Taking into account the defects indicated above, one has the following reaction equations:

$$0 = e' + h^{\cdot} : E_i \quad \ldots\ldots\ldots\ldots\ldots \tag{3.1}$$

$$0 = V_{Ga}^{x} + V_{As}^{x} \; ; \; H_s \quad \ldots\ldots\ldots\ldots \tag{3.2}$$

$$2V_{Ga}^{x} = (V_{Ga})_2^{x} \; ; \; H_p \quad \ldots\ldots\ldots\ldots \tag{3.3}$$

$$V_{Ga}^{x} = V_{Ga}' + h^{\cdot} \; ; \; E_a \quad \ldots\ldots\ldots\ldots \tag{3.4}$$

$$V_{As}^{x} = V_{As}^{\cdot} + e' \; ; \; E_b \quad \ldots\ldots\ldots\ldots \tag{3.5}$$

$$(V_{Ga})_2^{x} = (V_{Ga})_2' + h^{\cdot} \; ; \; E_{2a} \quad \ldots\ldots\ldots \tag{3.6}$$

$$1/2\ As_2(g) = As_{As}^{x} + V_{Ga}^{x} \; ; \; H_{As_2v} \ldots \tag{3.7}$$

Reactions (1-6) occurs in the solid phase. Reaction (7) represents transfer of arsenic atoms between the solid and gas phases. The energy and enthalpies of reaction are indicated on the right handside. The symbol H indicating enthalpy is used for reactions where a significant volume change may be involved. The mass action relations corresponding to the above reactions are as follows:

$$np = K_i \; ;$$

$$K_i = 1.0\text{x}10^{-12}\ T^3\ \exp(-1.88\text{x}10^4/T) \tag{3.8}$$

$$[V_{Ga}^{x}][V_{As}^{x}] = K_s \; ;$$

$$K_s = 1.15\text{x}10^4\ \exp(-4.64\text{x}10^4/T) \tag{3.9}$$

$$[V_{Ga}']p/[V_{Ga}^{x}] = K_a \ ;$$

$$K_a = 9.6\times10^{-8}\ T^{3/2}\ \exp(-510/T) \qquad (3.11)$$

$$[V_{As}]n/[V_{As}^{x}] = K_b \ ;$$

$$K_b = 4.9\times10^{-9}\ T^{3/2}\ \exp(-70/T) \qquad (3.12)$$

$$[(V_{Ga})_2']p/[(V_{Ga})_2^{x}] = K_{2a} \ ;$$

$$K_{2a} = 9.6\times10^{-8}\ T^{3/2}\ \exp(-510/T) \qquad (3.13)$$

$$[As_{As}^{x}][V_{Ga}^{x}]/P_{As_2}^{1/2} = K_{As_2v} \ ;$$

$$K_{As_2v} = 3.8\times10^{-4}\ \exp(-6650/T) \qquad (3.14)$$

Square brackets are used to indicate concentrations. As_{As}^{x} represents the concentration of arsenic atoms on arsenic sites and will be taken as unity. The partial pressure of As_2 in the gas phase is denoted by P_{As_2}. The equilibrium constant appearing on the right hand site of equations (8-14) have the general form:

$$K\ \exp(S/k)\ \exp(-H/kT) = K_o\exp(-H/kT) \qquad (3.15)$$

where S and H are the entropy and enthalpy changes of the reaction. K_o refered to as the pre-exponential factor.

The electroneutrality condition is obtained from Poisson's equation.

$$n + V_{Ga}' + (V_{Ga})_2' = p + V_{As}^{\cdot} \qquad (3.16)$$

Equations (3-8) to (3-16) represent eight equations for eight unknowns, and one can solve for these eight unknowns in terms of P_{As_2} and the temperature.

Thus, it is possible to obtain the concentration of gallium vacancies or arsenic vacancies from the above equations for a specific arsenic partial pressure and growth temperature.

IV. PREPARATION OF GaAs SAMPLES

The gallium-arsenide specimens used in this study were prepared by the VPE, LPE, and LEC techniques. Four n-type GaAs epitaxial samples were grown on semi-insulating Cr-doped GaAs substrates by Dr. R. Y. Loo, of Hughes Research Lab., using infinite solution melt liquid phase epitaxy (LPE) technique. The growth temperatures for these samples were held at 700°C and 800°C with temperature drop rates at 1°C/min. and 0.4°C/min., respectively. Schottky barrier diodes were fabricated from these LPE GaAs samples, for the DLTS and C-V measurements. In addition, van der Pauw test structures were also fabricated from these n-GaAs LPE layers for the resistivity and Hall effect measurements.

The VPE GaAs epitaxial layers used in this study were grown by Dr. P. C. Colter, at Air Force Avionics Lab., using a novel $Ga/AsCl_3/H_2$ reactor system [1]. The basic design of this reactor is like the usual two bubbler $AsCl_3$ reactor used for the MESFET growth [1]. The novel feature of this reactor is the addition of a third bubbler which feeds a cracking furnace and then a second source chamber to allow operation in a GaCl rich mode. It uses a six zone clamshell furnace which rolls off sideways allowing an end to end gas flow system. The third or control bubbler feeds a cracking furnace that is maintained at 900°C. The VPE GaAs epitaxial layers were grown on <100>, <211A>, and <211B> oriented semi-insulating Cr-doped GaAs substrates with growth temperatures ranging from 710 to 750°C. To facilitate the study of the effects of Ga/As ratio, substrate orientation, and growth temperature on the grown-in defects in the VPE GaAs epilayers, seven growth runs were made to prepare fourteen specimens for our study. The gas phase stoichiometry was controlled by varying the Ga/As ratio

from 2/1, 3/1, 4/1, 5/1, to 6/1. Au-GaAs Schottky barrier structure was fabricated from these VPE GaAs epilayers for the DLTS and C-V measurements. Room temperature resistivity and Hall effect measurements were also performed on these epilayers to determine the carrier concentration and electron mobility in these samples.

Finally, several Al-P-GaAs Schottky barrier diodes were fabricated from the p-GaAs specimens grown by the liquid encapsulated Czochralski technique for the purpose of studying the unknown native defects in these samples.

V. RESULTS OF RESISTIVITY AND HALL EFFECT MEASUREMENTS

In order to obtain the information on the carrier concentration and mobility in the GaAs samples, the resistivity and Hall effect measurements were performed on the LPE GaAs specimens for temperature between 80 K and 300 K and on the VPE GaAs samples for T = 300 K. Resistivity, carrier density and electron mobility were deduced from these measurements, and the results are shown in Fig. 5.1 through Fig. 5.4, Table 5.1, and Table 5.2. Fig. 5.1 shows the resistivity vs. temperature plot for three LPE GaAs samples grown at 700 and 800°C with temperature drop rates of 0.4 °C/min. and 1°C/min. As noted in this figure, the sample grown at 700°C with 1°C/min. temperature drop rate has the lowest resistivity while sample grown at 700°C with 0.4°C/min. drop rate has the highest resistivity. Fig. 5.2 shows the Hall mobility vs. temperature for three LPE GaAs samples shown in Fig. 5.1; the Hall mobility at 300 K is around 5000 $cm^2/V_.s$ and increases to around 28000 $cm^2/V_.s$ at 80 K for sample grown at 700°C with 0.4°C/min. drop rate has the lowest mobility at 80 K. Fig. 5.3 shows the carrier density vs. inverse kT plot for the same samples shown in Fig. 5.1; the results show that electron concentration for these LPE GaAs samples is in the mid 10^{15} cm^{-3} to low 10^{16} cm^{-3} range at T = 300 K. Sample grown at 700°C with 0.4°C/min. drop rate has the lowest carrier density while sample grown at 700°C with 1°C/min. drop rate has the highest carrier density. This result may be attributed to the fact that increasing cooling rate during the growth of GaAs LPE layer tends to increase native defect density as is evidenced by the DLTS data to be discussedin section 7.0.

Table 5.1 summarizes the measured transport data at 300K for the three LPE GaAs samples shown in Fig. 5.1 through Fig. 5.3. Resistivity and Hall effect measurements on the VPE GaAs specimens with different substrate orientations and Ga/As ratios were made at 300 K. The results are summarized in Table 5.2 in which carrier density and electron mobility were listed for several VPE GaAs samples with <211A> and <100> orientations and with Ga/As ratios equal to 3/1 and 6/1. Fig. 5.4 shows the electron concentration as a function of the distance from the epilayer surface of the VPE GaAs samples. The carrier concentration remains essentially constant for epilayer depth greater than one μm. Not that samples 35CA and 35CB are prepared under the same growth conditions so are samples 37HB and 37HA. It is interesting to note that sample grown on <100> substrate orientation has in general a lower carrier density than those of <211A> oriented samples grown under identical condition. It was found that sample 39HB <211A> has the lowest carrier density among all the samples studied in this work. In fact, it has also the lowest grown-in defect density as will be shown later in section 7.0. The electron mobility for this sample is around 6000 $cm^2/V_{-}s$ at 300 K, which is about 10% higher than the rest of samples studied. It will be shown in section 7.2 that high purity (or low carrier concentration) sample has also low density of grown in defects,and it appears that there is a direct correlation between the intrinsic defect density and background density in the samples studied.

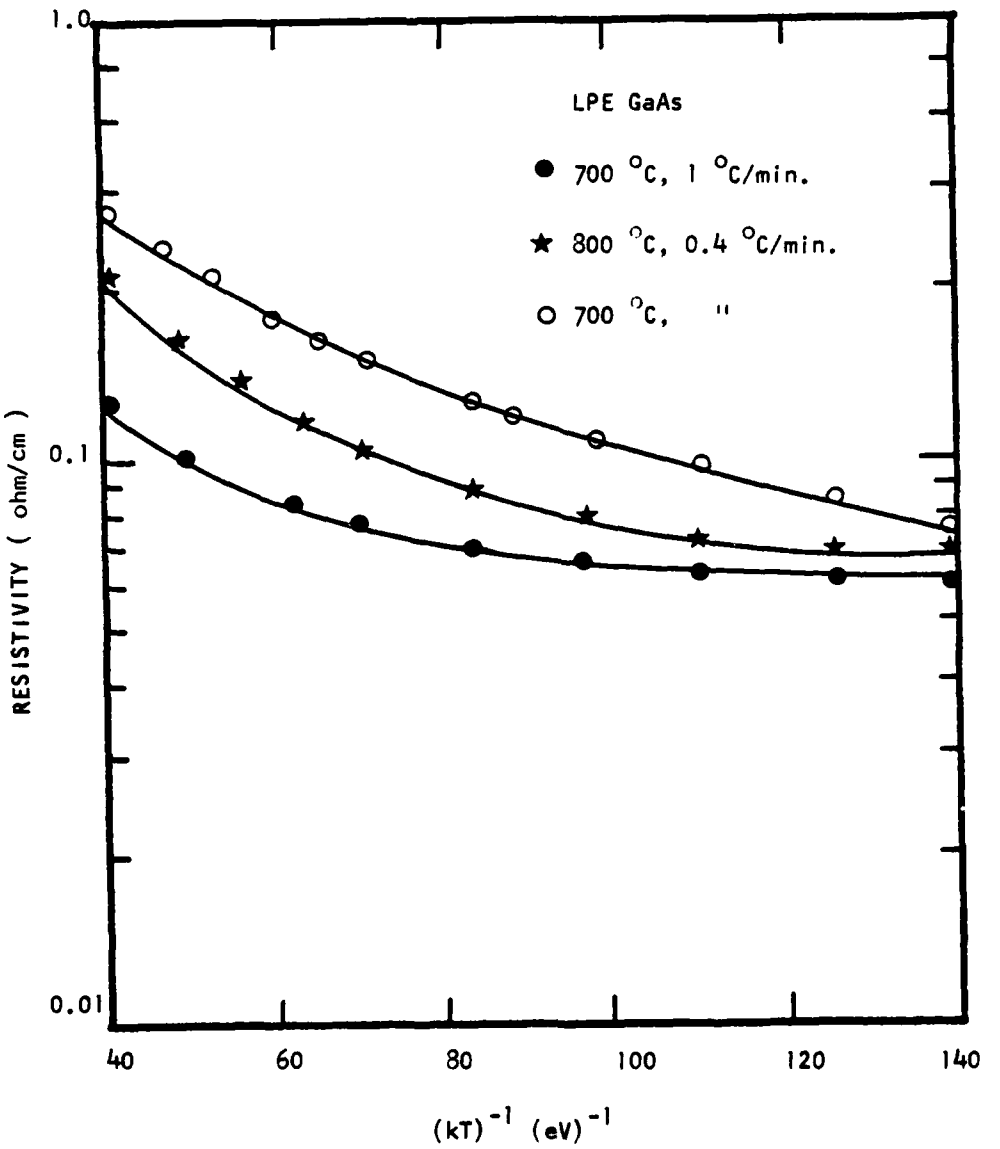

Fig. 5.1 Resistivity vs $(kT)^{-1}$ for three LPE GaAs samples with growth temperature and growth cooling rate as parameters

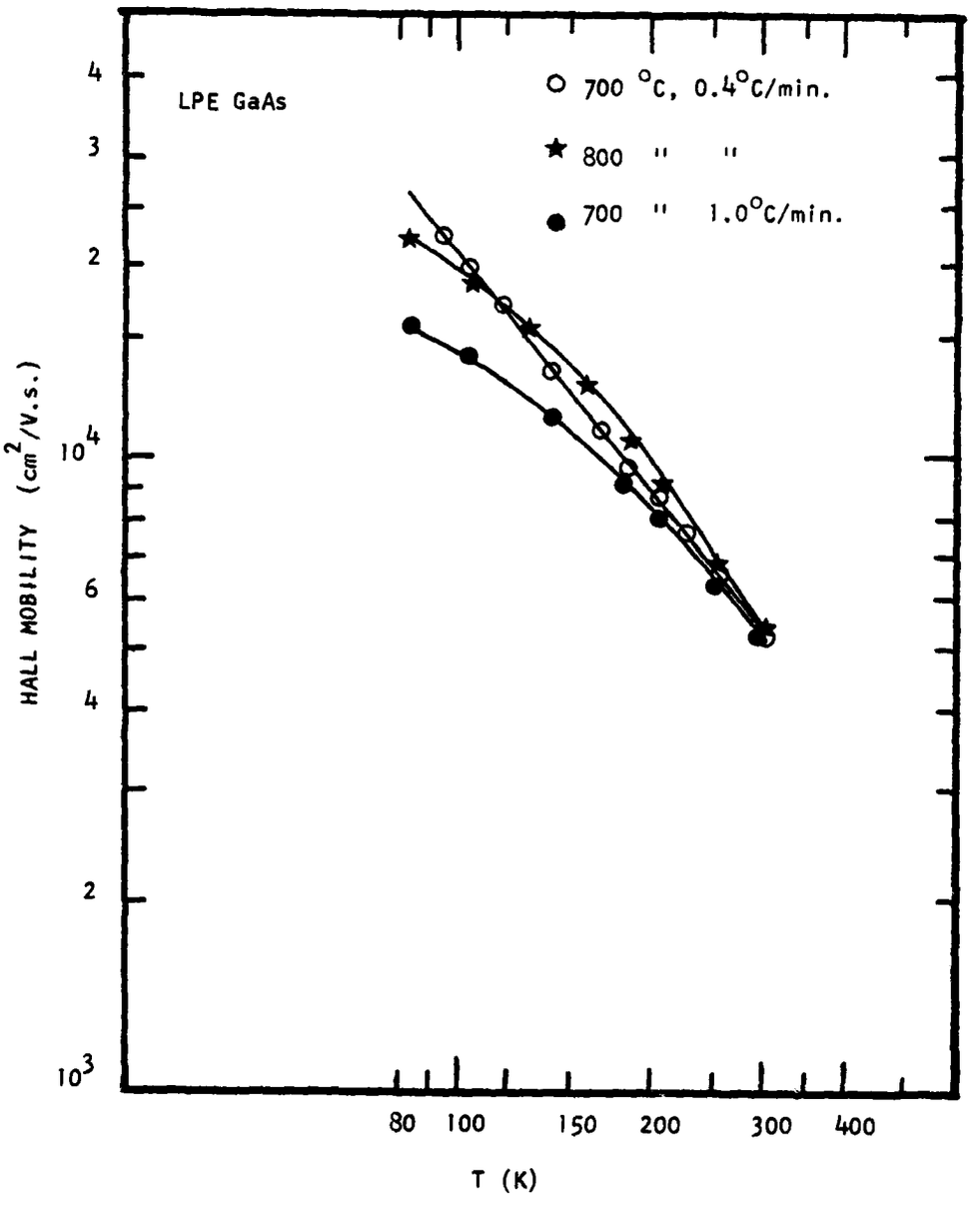

Fig. 5.2 Hall mobility vs temperature for three LPE GaAs samples with growth temperature and cooling rate as parameters.

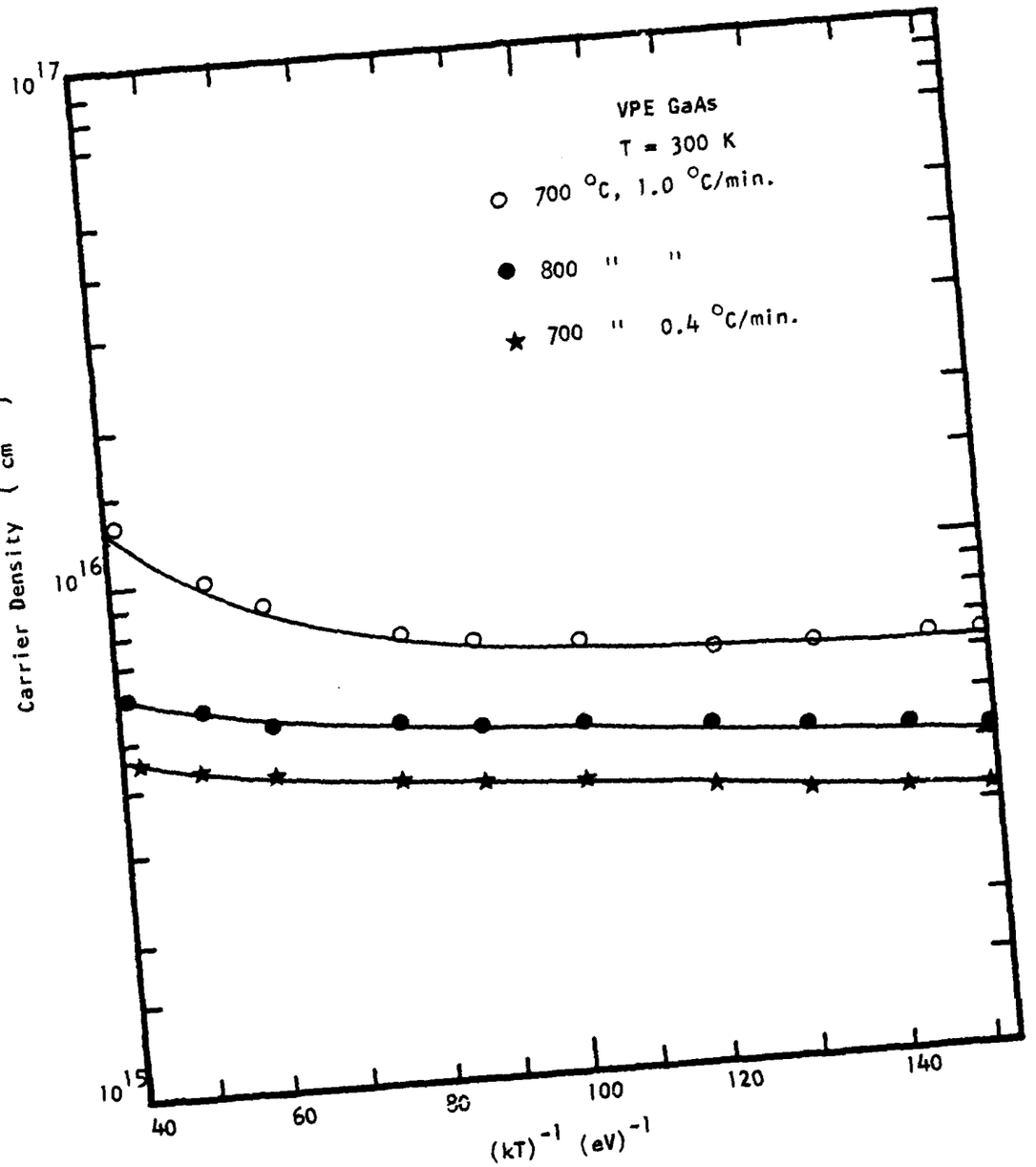

Fig. 5.3 Carrier density vs $(kT)^{-1}$ for three LPE GaAs samples with Growth temperature and cooling rate as parameters.

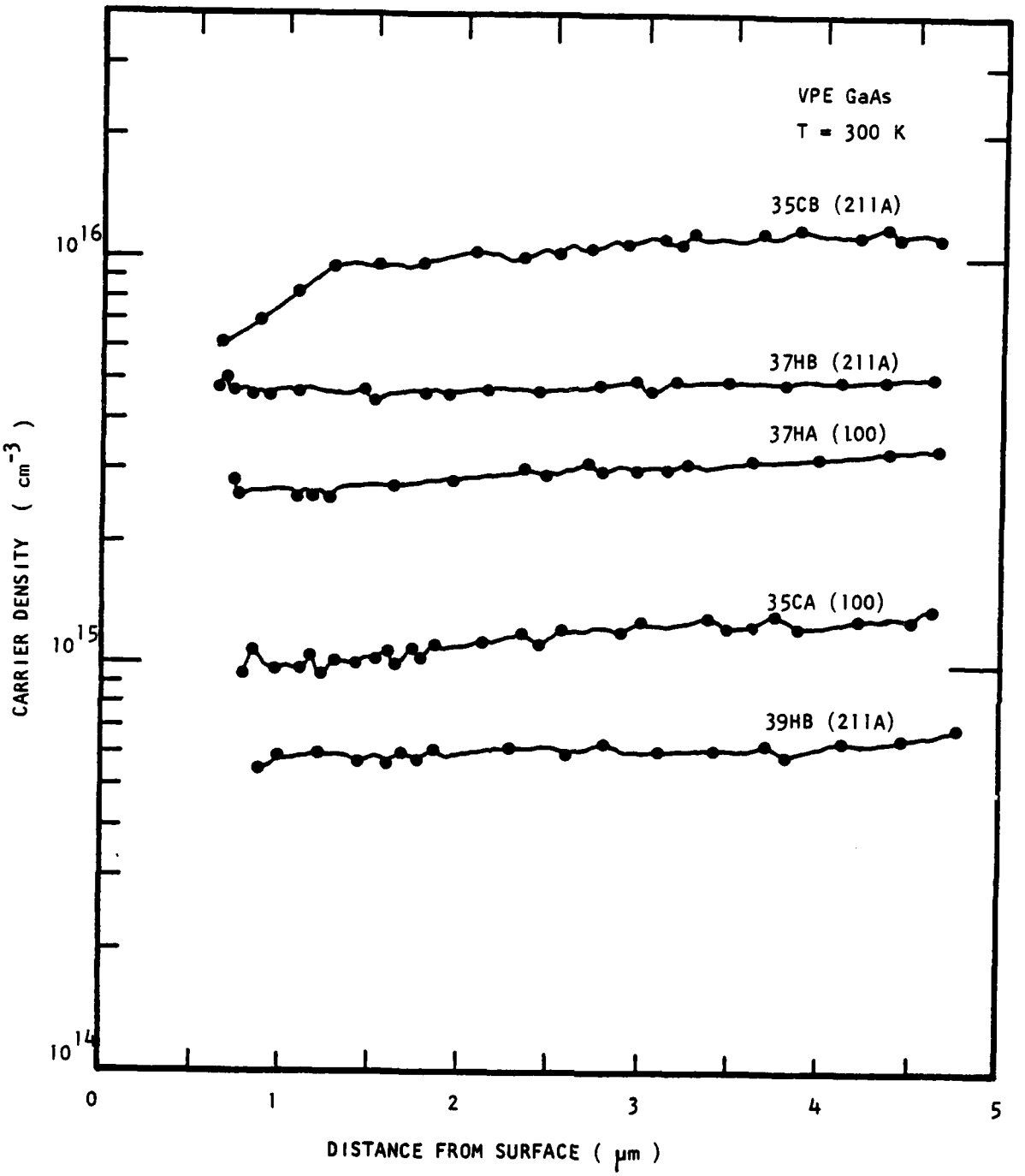

Fig. 5.4 Carrier density vs distance from surface of five VPE GaAs samples of different substrate orientations.

Table 5.1 Transport parameters in LPE GaAs Samples
(296 K)

Samples No.	Carrier concentration (cm^{-3})	Electron Mobility ($cm^2/v \cdot s$)	Resistivity (Ω-cm)	Growth Temp. (°C)	Cooling Rate
LEPI-43 (5μ layer)	5.26×10^{15}	5.42×10^{3}	0.2189	800	0.4°C/min.
LEPI-44 (7.5μ layer)	7.63×10^{15}	5.03×10^{3}	0.1627	800	1°C/min.
LEPI-45 (2μ layer)	4.05×10^{15}	5.05×10^{3}	0.2745	700	0.4°C/min.
LEPI-46 (3μ layer)	9.26×10^{15}	5.36×10^{3}	0.1259	700	1°C/min.

Table 5.2 Transport Parameters in GaAs VPE Samples (T = 296 K)

Samples No. (orientation)	Carrier density (cm^{-3})	Electron Mobility ($cm^2/v \cdot s$)	Ga/As Ratio
RR35CA (100)	1.2×10^{15}	5.7×10^{3}	3/1
RR35CB (211A)	1.1×10^{16}	5.6×10^{3}	3/1
RR37HA (100)	3.09×10^{15}	5.36×10^{3}	6/1
RR37HB (211A)	5.16×10^{15}	5.59×10^{3}	6/1
RR39HB (211A)	7.1×10^{14}	5.96×10^{3}	6/1
RR57HB (211A)	5×10^{15}	5.45×10^{3}	3/1

VI. RESULTS OF THE C-V AND TSCAP MEASUREMENTS

The capacitance-voltage (C-V) measurement can be used to determine the background doping concentration in the n- or p- GaAs epitaxial layers using the Schottky barrier structures. Since the Schottky barrier diode can be considered as a one-sided abrupt p^+-n (or n^+p) junction, the depletion capacitance across the Schottky barrier diode is given by:

$$C = \frac{\epsilon_s A}{W} = A\left[\frac{q\epsilon_s N_D}{2(\phi_i \pm V_a - kT/q)}\right]^{1/2} \tag{6.1}$$

where A is the area of the diode, ϕ_i is the built-in potential, V_a is the applied voltage, and N_D is the background doping density. Eq. (6.1) shows that the depletion capacitance of a Schottky diode is directly proportional to the square root of dopant density and inversely proportional to the square root of the applied voltage. If the inverse of capacitance square (C^{-2}) is poltted a function of the reverse bias voltage, V_a, then the background dopant density, N_D, can be calculated from the slope of C^{-2} vs. V_a, using the following expression:

$$C^{-2} = \left(\frac{2}{q\epsilon_s A^2 N_D}\right)(\phi_i + V_a) \tag{6.2}$$

The intercept of C^{-2} vs. V_a plot with the voltage axis yields values of ϕ_i which is related to the barrier height of the Schottky diode by:

$$\phi_{Bn} = \phi_i + V_n + kT/q - \Delta\phi \tag{6.3}$$

where
$$V_n = E_c - \left(\frac{kT}{q}\right) \ln (N_D/N_C) \tag{6.4}$$

and $\Delta\phi$ is the image lowering potential.

If the barrier lowering potential is neglected, then the barrier height, ϕ_{Bn}, can be determined from the C-V measurement. The results of our C-V measurements for the VPE GaAs samples are discussed next. The C-V measurements on the GaAs Schottky diodes were carried out by using a PAR model-410 C-V plotter and a HP-7010A x-y recorder. A typical C-V plot for a VPE GaAs Schottky diode is shown in Fig. 6.1. Fig. 6.2 shows the C^{-2} vs. V_a plots for six VPE GaAs Schottky diodes fabricated under different growth conditions and substrate orientations. It is noted that a linear relationship exists between C^{-2} vs. V_a for all the diodes shown with the intercept around $V_a = \phi_i = 0.83$ to 0.88 eV. The Schottky barrier height, ϕ_{Bn}, deduced from the C^{-2} vs. V_a plot for these gold-n-GaAs Schottky diodes, was around 1 eV, in good agreement with the published data for the barrier height of the Au-n GaAs Schottky diode. Table 6.1 lists the calculated values of N_D, ϕ_i, V_n, and ϕ_{Bn} from the C-V data for the VPE GaAs samples shown in Fig. 6.2. The background carrier concentration was found to vary from mid 10^{14} cm^{-3} to low 10^{16} cm^{-3}. Note that the carrier concentration for <100> oriented VPE GaAs samples was found lower by a factor of two to five than that of <211> oriented VPE GaAs samples. A similar trend was also found for the density of grown-in defects in the (100) and (211) samples. Note that analysis of the C-V data for the LPE GaAs and LEC GaAs samples was also performed, and the results are being incorporated in the DLTS analysis to be discussed in section 7.2.

Another interesting experiment, which is known as the thermally stimulated capacitance (TSCAP) measurement technique [17-18], has also been used to study the deep-level traps in the LEC GaAs samples. The TSCAP experiment is carried out by first reverse biasing the p-n diode or the Schottky diode and then

cooling down the diode to liquid nitrogen temperature; the diode is then momentarily zero biased to fill the majority carrier traps and subsequently returned to zero bias condition; the diode is then heated to raise the temperature from 77 K to 300 K; the thermal scan of the capacitance (at 1 MHz) vs. temperature plot is then taken by an x-y recorder; a capacitance step is seen from the C vs. T plot if majority or minority carrier emission is taking place from a trap level. The amplitude of this capacitance step is directly related to the trap density. The trap density for n-type GaAs can be calculated from the following expression:

$$N_T = N_D \left(\frac{2\Delta C}{C_o}\right) \tag{6.5}$$

where N_D (or N_A) is the background carrier density; C_o is the depletion layer capacitance and ΔC is the capacitance change due to the majority or minority carrier emission. Thus, knowing N_D (or N_A) and C_o at the temperature where the capacitance step observed, the density of the trap can be calculated from Eq. (6.5). Note that Eq. (6.5) is valid only for the case when $N_T \leq 0.1\ N_D$. Fig. 6.3 shows the TSCAP scan for an Al-p-GaAs Schottky diode grown by LEC technique. A large capacitance step was seen in the Figure in the temperature range from 125 to 150 k; this capacitance change was a direct result of the hole emission from a hole trap located at E_v+0.080 eV. Following this hole trap level, another capacitance step was also observed between 150 to 200 k due mainly to an electron trap located at E_c-0.18 eV. Both of these two levels were also observed in the DLTS and photoluminescence measurements as will be discussed in section 7.0. Although the TSCAP experiment cited above can be used to determine the trap density in a Schottky diode or a p-n junction diode, the technique is not very sensitive and has been replaced by the DLTS technique more recently for studying the deep level traps in semiconductors. This capacitance transient spectroscopy technique will be described next.

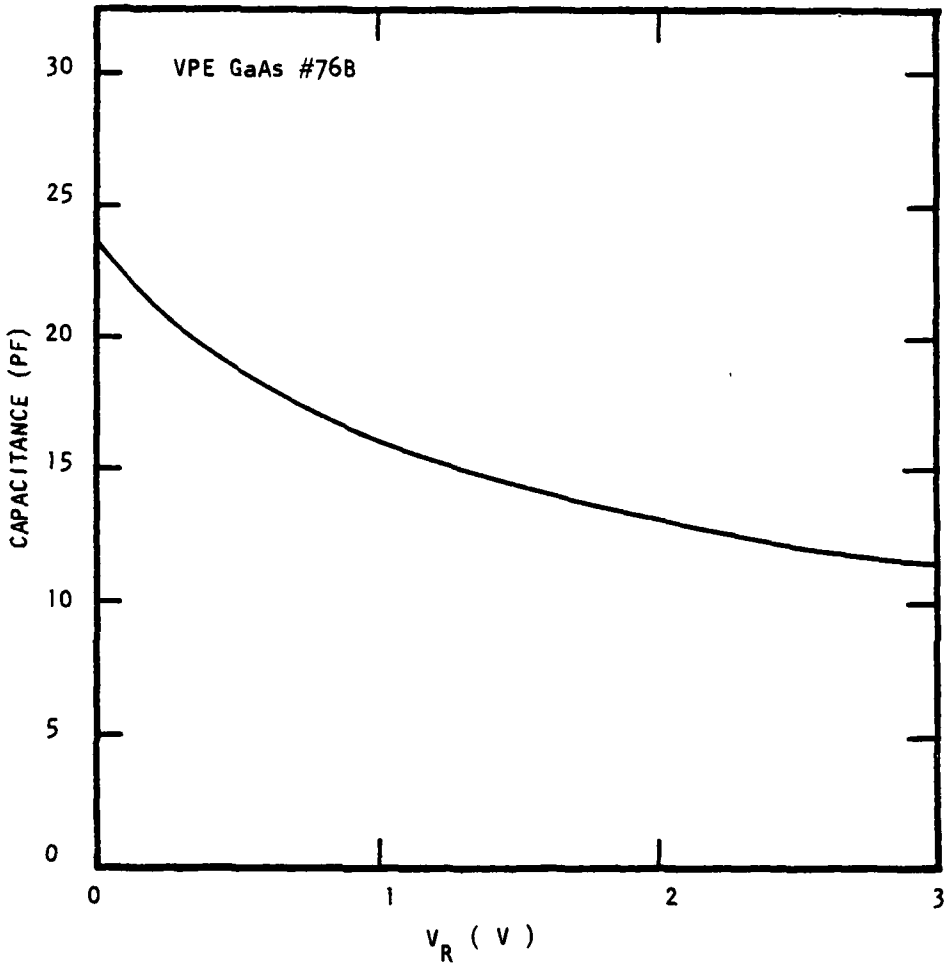

Fig. 6.1 Capacitance vs voltage for an n-GaAs VPE sample.

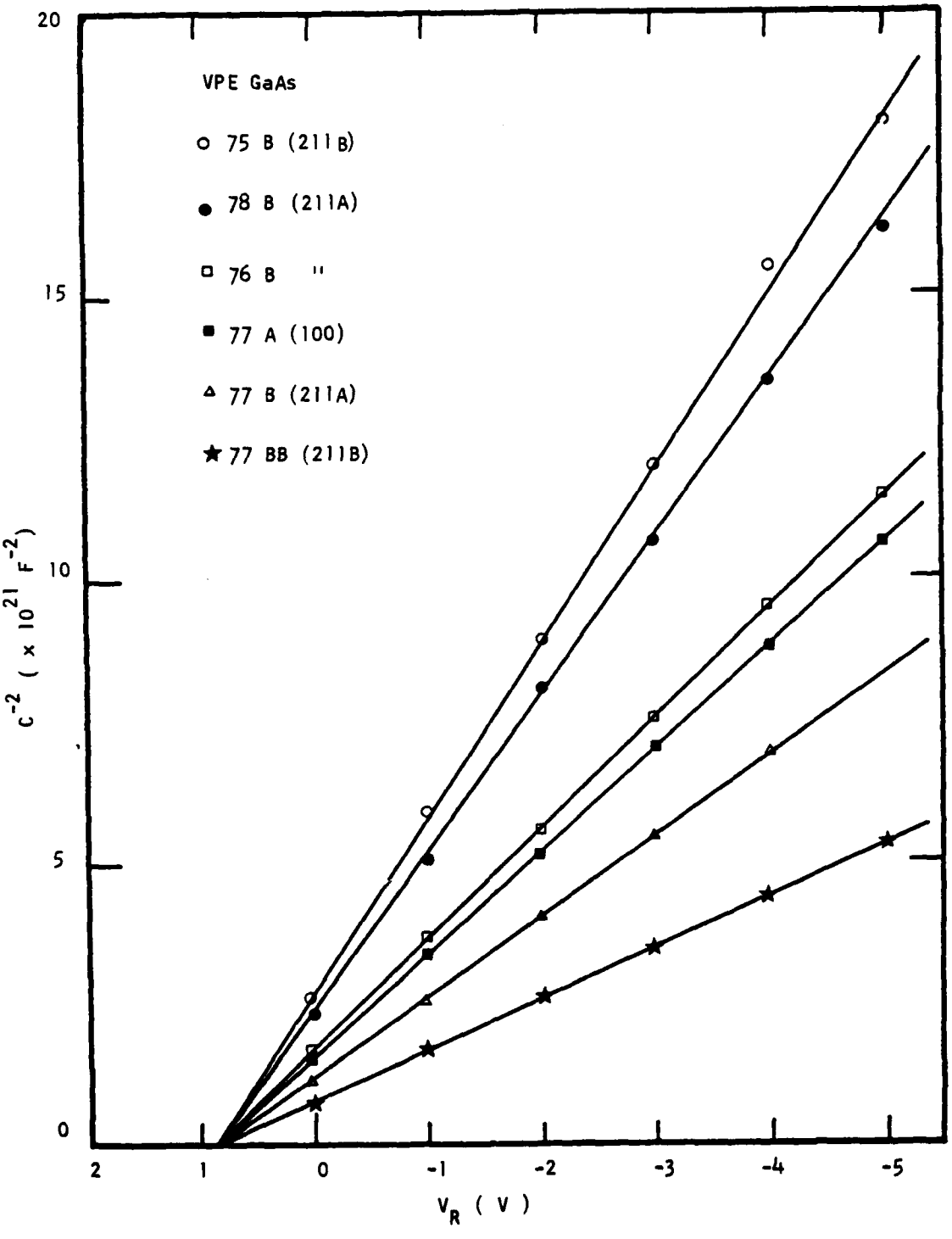

Fig. 6.2 Inverse capacitance square vs V_R for six VPE GaAs samples.

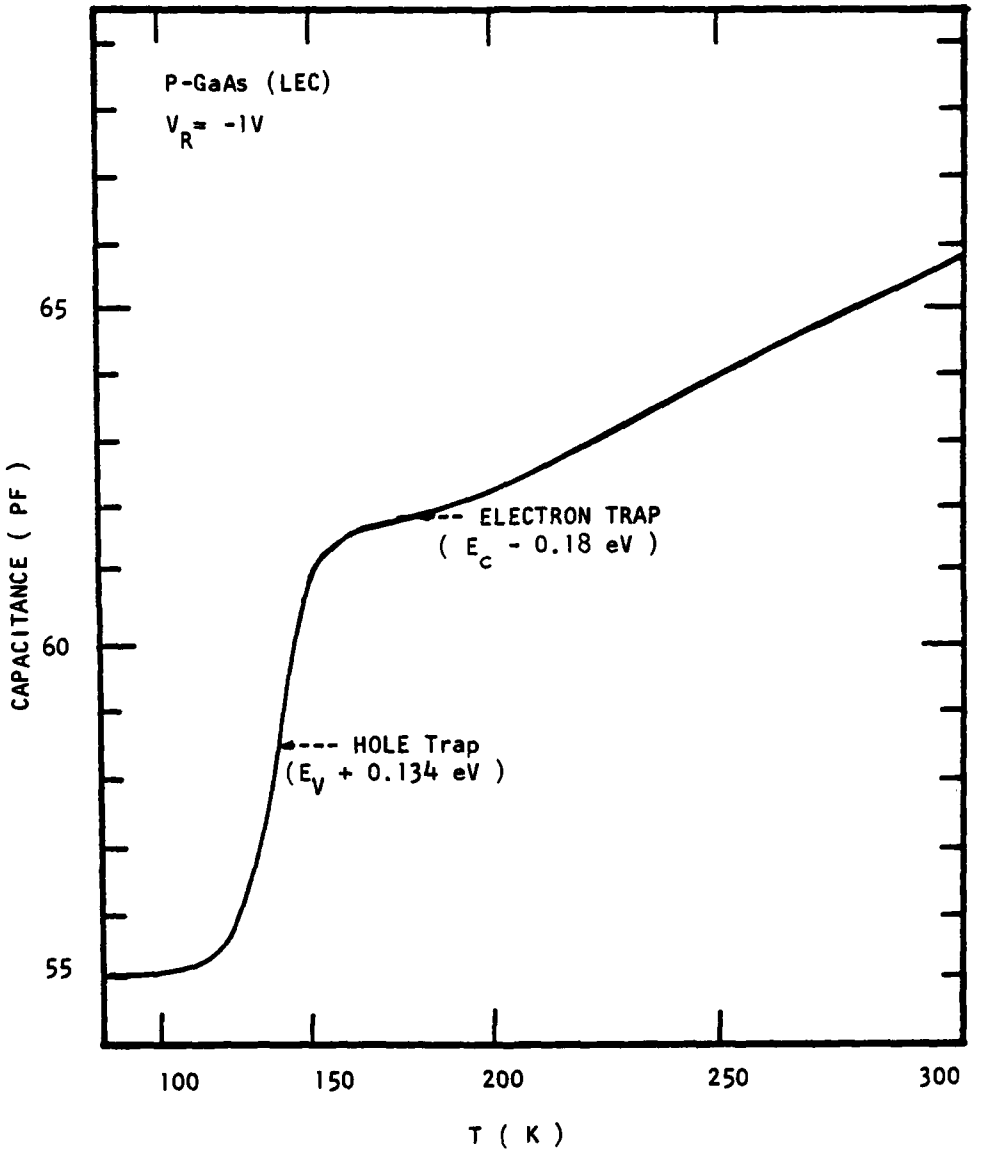

Fig. 6.3 Thermally Stimulated Capacitance (TSCAP) measurements of trap levels in LEC grown p-GaAs sample.

Sample	Orientation	Ga/As Ratio	$N_D(cm^{-3})$	ϕ_i (V)	V_n (V)	ϕ_{Bn}^* (V)
35CA	100	2/1	$6.7x10^{14}$	0.83	0.17	1.0
35CB	211A	2/1	$1.7x10^{15}$	0.83	0.15	0.98
37HA	100	6/1	$1.3x10^{15}$	0.83	0.15	0.98
37HB	211A	6/1	$3.1x10^{15}$	0.87	0.13	1.0
75A	100	3/1	$7.2x10^{14}$	0.83	0.17	1.0
75B	211B	3/1	$3.x10^{15}$	0.87	0.13	1.0
76A	100	4/1	$3.x10^{15}$	0.87	0.13	1.0
76B	211A	4/1	$5.5x10^{15}$	0.88	0.12	1.0
77A	100	4/1	$1.x10^{15}$	0.83	0.16	0.99
77B	211A	4/1	$7.2x10^{15}$	0.87	0.11	0.98
77BB	211B	4/1	$5.6x10^{15}$	0.88	0.12	1.0
78B	211A	5/1	$3.8x10^{15}$	0.86	0.13	0.99
78BB	211B	5/1	$1.x10^{16}$	0.88	0.1	0.98

Table 6.1 Background concentration, N_D, and barrier height, ϕ_{Bn}, in the n-GaAs VPE samples.

VII. RESULTS AND DISCUSSIONS OF THE DLTS MEASUREMENTS

The Deep-Level-Transient Spectroscopy (DLTS) experiment is a high frequency (i.e., 20 MHz or higher) transient capacitance spectroscopy technique, which was introduced first by Lang in 1974 [22-23]. The DLTS scan displays the spectrum of deep level traps in the forbidden gap of a semiconductor as positive or negative peaks on a flat baseline as a function of the temperature. Although the DLTS measurement is time consuming, it offers several advantages over the conventional TSCAP technique described in the preceding section. The DLTS technique is sensitive, easy to analyze, and capable of measuring traps over a wide range of depth.

The DLTS system consists of a sensitive capacitance measurement apparatus with transient response, a pulse generator, a boxcar averager with dual-gated signal integrators, an x-y recorder, and a cryostat for temperature controlling use. By properly monitoring the experimental parameters it is possible to determine the following defect parameters from the DLTS measurements:

- The majority and minority carrier traps.
- The activation energy of each trap level.
- The defect concentration.
- The defect concentration profile.
- The capture cross sections of electrons and holes in each trap level.

Theoretical aspects of the DLTS technique, and the results of our DLTS measurements on the VPE, LPE, and LEC GaAs specimens are discussed separately in section 7.1 and section 7.2.

7.1 Principles of the DLTS Technique

The capacitance transient is associated with the return to thermal equilibrium of the occupation of the trap level following an initial nonequilibrium condition. The polarity* of the peak depends on the capacitance change after trapping the minority or majority carriers. Because an increase in trapped minority carriers in the junction space charge region causes an increase in the junction capacitance, the minority carriers trapping will result in a positive polarity peak in the DLTS scan. For example, in a p^+-n junction diode, the space charge region extends mainly into the n-type region and the local charges are due to positively charged ionized donors. If a forward bias is applied, the minority carriers (holes) will be injected into this region. Once the holes are trapped in the defect levels the net positive charges in the space charge region will increase. This results in a narrower space charge region width which implies a positive capacitance change. Therefore, the peak is positively polarized. Similarly, if the majority carriers are injected into this region and captured by the majority carrier traps, which reduces the local charges, the space charge region width will be widened, implying a decrease of the junction capacitance. Therefore, the majority carriers trapping will result in a negative polarity peak in the DLTS scan. The same argument can be applied to the n^+-p junction diodes. All of the VPE and LPE GaAs samples used in these measurements are Au-n GaAs Schottky diodes so that the positive peak represents the hole trap, and the negative peak represents the electron trap. For the LEC p-GaAs Schottky diodes, the polority of the DLTS scans is opposite to those VPE or LPE samples.

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*positive polarity means the peak is convex; negative polarity means the peak is concave

7.1.1 Minority Carriers Injection

Figure 7.1 shows the injection of minority carriers. Figure 7.1(a) is the injection pulse where $V=V_p>0$ during the pulse ($t_a \leq t \leq t_b$) and $V=V_R \leq 0$ outside the time interval (t_a, t_b). Figure 7.1(b) is a simplified energy band diagram (the band bending due to the junction electric field is omitted) in quiescent reverse bias condition ($t<t_a$). Figure 7.1(c) is the saturating injection pulse ($t_a \leq t \leq t_b$). During the pulse the minority carrier traps E_t are filled by holes. Figure 7.1(d) shows the transient ($t>t_b$); the trapped holes begin to emit from the trap centers to valence band and then swept out of the space charge region by the built-in electric field that causes the capacitance transient.

7.1.2 Majority Carriers Injection

Figure 7.2 shows the injection of the majority carriers. Figure 7.2(a) is the injection pulse where $V=V_p=0$ during the pulse ($t_a \leq t \leq t_b$) and $V=V_R<0$ outside the time interval (t_a, t_b). Figure 7.2(b) is a simplified band diagram in quiescent reverse bias condition ($t<t_a$). Figure 7.2(c) is the majority carriers injection. During the pulse period ($t_a \leq t \leq t_b$), the majority carriers were injected into the space charge region and captured by the majority trap centers. Figure 7.2(d) is the transient ($t>t_b$); the captured electrons begin to emit from the trap centers to conduction band and then swept out of the space charge region by the built-in electric field that causes the capacitance transient.

7.1.3 Defect Concentration

The defect concentration is directly proportional to the peak height as

described before, and the peak height is proportional to the capacitance change ΔC (ΔC is shown in Figure 7.1(d) and 7.2(d)). Therefore, the defect concentration N_t is proportional to ΔC as follows:

$$C(t) = \sqrt{q\varepsilon_s (N_D-N_t)/2(V_{bi}+V_R)}$$

$$= C_o(1-N_t/N_D)^{1/2} \qquad (7.1)$$

where $C_o = C(V_R) = \sqrt{q\varepsilon_s N_D /2(V_{bi}+V_R)}$ is the junction capacitance at the quiescent reverse bias condition. Using binomial expansion and the condition that $N_t/N_D \ll 1$, Eq. (7.1) reduces to a simple form as:

$$C(t) \cong C_o(1-N_t(t)/2N_D) \qquad (7.2)$$

This can be rewritten as

$$N_t = (2\Delta C/C_o)N_D \qquad (7.3)$$

where $\Delta C = C_0-C(t)$. From the DLTS measurement, ΔC can be determined. The junction capacitance C_o and the background concentration N_D can be obtained from the C-V measurements. Thus, the defect concentration N_t can be calculated easily by using Eq. (7.3).

7.1.4 Activation Energy of the Defect Level

As shown in Fig. 7.3, ΔC begins to decay after the injection pulse is over. The decay is associated with a specific time constant τ which is the reciprocal of the emission rate. For an electron trap, the emission rate is functions of temperature, capture coefficient, and activation energy, and can be expressed by:

$$e_n = (\sigma_n \langle V_{th} \rangle N_c/g)\exp(-E_T/kT) \qquad (7.4)$$

where σ_n is the electron capture cross section, $\langle V_{th} \rangle$ is the average thermal

velocity of electron, N_c is the effective conduction band states, g is the degeneracy factor, and E_T is the activation energy of the trap. If the electron capture cross section σ_n is independent of temperature, e_n can be expressed as:

$$e_n = BT^2 \exp(-E_T/kT) \tag{7.5}$$

where B is the proportionality constant and is independent of temperature. From this expression it is seen that e_n increases exponentially with temperature. The capacitance transient is given by:

$$C(t) = \Delta C(0) \exp(-t/\tau) \tag{7.6}$$

where $\tau = e_n^{-1}$.

The procedures to deduce the activation energy of a defect level from the DLTS measurements are discussed next. The t_1 and t_2 were setting by the dual-gated boxcar averager, then

$$C(t_1) = \Delta C \exp(-t_1/\tau) \tag{7.7}$$

$$C(t_2) = \Delta C \exp(-t_2/\tau) \tag{7.8}$$

The DLTS signal is obtained by taking the difference of Eq. (7.7) and (7.8), which yields

$$\begin{aligned} S(T) &= \Delta C \exp(-t_1/\tau) - \Delta C \exp(-t_2/\tau) \\ &= \Delta C[\exp(-t_1/\tau) - \exp(-t_2/\tau)] \end{aligned} \tag{7.9}$$

Differentiating S(T) in Eq. (7.9) with respect to τ and letting it equal to zero, gives:

$$\tau = \tau_{max} = (t_1 - t_2)/\ln(t_1/t_2) \tag{7.10}$$

Under this condition, S(T) reaches its maximum value at a specific temperature. The emission rate is given by $e_n = 1/\tau_{max}$ for each t_1 and t_2 setting. By

changing t_1 and t_2 several times, a set of temperatures corresponds to this set of τ_{max} (or emission rate e_n) can be obtained as shown in Fig. 7.3. From the Arrhenius plot of emission rate (i.e., $\ln(e_n/T^2)$ vs. $1/kT$), the activation energy of the trap can be calculated from the slope of this plot.

7.2 Results and Discussions

In this section we discuss the results of our DLTS and C-V analysis of the grown-in deep level defects in the GaAs specimens grown by the VPE, LPE, and LEC techniques under various growth conditions. Defect parameters such as defect energy level, defect density and capture cross section were deduced from the DLTS and C-V data. The results are presented separately in the following subsections.

7.2.1 VPE n-GaAs Samples

In this section, we present the results of our DLTS and C-V measurements on the VPE GaAs samples described in section 4.0. The DLTS scans of electron traps as a function of Ga/As ratio for different runs and substrate orientations are shown in Fig. 7.4 through Fig. 7.12. Fig.7.4 shows the DLTS scans of electron traps as a function of the Ga/As ratio, for samples with <211A> orientation. In general, one to two electron traps (i.e., EB4 = E_c-0.71 eV, and EL2 = E_c-0.83 eV) were observed in these samples. Note that sample 37HB with the highest Ga/As ratio (i.e., 6/1) has the lowest density for EL2 electron trap, while sample 35CB with the lowest Ga/As ratio (i.e., 2/1) has the highest density of EL2 electron trap. Thus, for the <211A> oriented samples (i.e.,

Ga-rich face), the density for EL2 level decreases with increasing Ga/As ratio; this same trend was also observed in EB4 electron trap. Fig. 7.5 shows the DLTS scans of electron traps as a function of the Ga/As ratio for epilayers grown on the <100> oriented substrates. Results showed that the density of EL2 level may either increase or decrease with increasing Ga/As ratio, depending on the types of defects formed during the growth. To explain this, model proposed by Zou [29] appears to be adequate for this case. He suggested that EL2 level may be attributed to either the antisite defect of As_{Ga} or gallium di-vacancy defect, $(V_{Ga})_2$. If the EL2 level is due to the $(V_{Ga})_2$ defect, then the density of EL2 level should be decreased with increasing Ga/As ratio as is in the case of <211A> oriented samples shown in Fig. 7.4. On the other hand, if the EL2 level is due to the antisite defect of As_{Ga}, then increasing GaAs ratio will also increase the density of EL2 level; this is the case for <211B> oriented samples. The two defects model proposed by Zou for predicting the orientation dependence of the density of EL2 vs. Ga/As ratio, appears consistent with our experimental observation in the VPE GaAs samples as shown in Fig. 7.12. Fig. 7.6 shows the DLTS scans of electron traps for sample 35CA (100 orientation) and sample 35CB (211A) with Ga/As ratio equal to 2/1. These two samples were grow in the same run side by side at 715°C. The DLTS results showed that density of EL2 electron trap for the <211A> samples is significantly higher than that of the <100> sample (i.e., 1.24×10^{14} cm^{-3} vs. 7.6×10^{12} cm^{-3}). The reason for this may be attributed to the fact that density of $(V_{Ga})_2$ is higher in the <211A> face than that in the <100> face for the Ga/As ratio equal to 2/1. The EB4 electron trap was not observed in both samples shown in Fig. 7.6. Fig. 7.7 shows the DLTS scans of electron trap for sample 75A <100> and sample 75B <211B> with Ga/As ratio equal to 3/1. Note

that the EL2 level was observed only in sample 75A while EB4 level was observed only in 75B sample. These two samples were also grown in the same run. The growth temperature for both samples was held at 725°C. Fig. 7.8 shows the DLTS scans of electron traps for samples 76A (100) and 76B (211A). The results showed that both EL2 and EB4 electron traps were observed in these two samples. Density of EL2 and EB4 levels was higher for sample 76B <211A> than sample 76A <100>. Fig. 7.9 shows the DLTS scans of electron traps for samples 77B (211A), 77A (100), and 77BB (211B). These three samples were grown side by side at 750°C and with Ga/As ratio equal to 4/1. Both EL2 and EB4 electron traps were observed in these three samples; the density of EL2 and EB4 levels was highest for sample 77BB, followed by samples 77B, and 77A. Fig. 7.10 shows the DLTS scans of electron traps for samples 78B (211A) and 78BB (211B) grown at 725°C and with Ga/As ratio equal to 5/1. The results showed that EL2 level was the dominant electron trap for sample 77BB while only EB4 level was observed in sample 78B. Fig. 7.11 shows the DLTS scans of electron traps for samples 37HA (100) and 37HB (211A) grown at 725°C and with Ga/As ratio equal to 6/1. The results showed that both EL2 and EB4 level was observed in sample 37HB. To sum up the results shown in Fig. 7.4 through Fig. 7.11 concerning the effects of orientation, Ga/As ratio, and the growth temperature on the density of EL2 and EB4 levels, we plot in Fig. 7.12 the density of EL2 level vs. Ga/As ratio for three substrate orientations. In Fig. 7.12, it is clearly shown that density of EL2 level was found to decrease with increasing Ga/As ratio for the <211A> oriented samples and to increase with increasing Ga/As ratio for the <211B> oriented samples; for the <100> oriented samples the density of EL2 level may increase or decrease with increasing Ga/As ratio, depending on the types of defects formed during the epilayer growth (i.e., $(V_{Ga})_2$ vs. As_{Ga} defect for EL2 level). Table 7.1 summarizes the defect

parameters deduced from our DLTS and C-V measurements fortwelve VPE GaAs samples prepared under different growth conditions and substrate orientations.

The EB4 level (i.e., E_c-0.71 eV) observed in our VPE GaAs samples might be due to the bound pairs of antisite defect, As_{Ga} Ga_{As}, which constitute a neutral defect. Based on the QDT (quantum dielectric theory) and those of Pauling's theory of electronegativities, the formation energy for the As_{Ga}-Ga_{As} should be around 0.70 to 0.72 eV. This antisite defect complex has been observed in the proton and electron irradiated LPE GaAs specimens. Thus, the activation energy for EB4 level deduced from the DLTS data for the VPE GaAs samples is in excellent agreement with the formation energy predicted for the As_{Ga} Ga_{As} defect. On the other hand, the EL2 electron trap (i.e., E_c-0.83 eV) is commonly seen in the VPE GaAs when growth conditions are made under arsenic-rich condition; the EL2 level is not normally observed in the LPE GaAs grown under gallium-rich condition. Several studies identify the EL2 level as gallium vacancy related defect [27,28]. In addition to $(V_{Ga})_2$ defect, EL2 has also been related to the antisite defect of As_{Ga}. Based on the defect model proposed by Zou [29] for EL2 level, the following relationship exists for the EL2 level: The gallium divacancy may be produced by the following reaction equation

$$\frac{P_{AsH_3}}{P_{GaCl}} \propto \frac{[V_{Ga}]}{[V_{As}]} \propto \frac{[V_{Ga}]^2}{[V_{Ga}]\,[V_{As}]} \propto [\,V_{Ga}]^2 \qquad (7.11)$$

while the gallium on arsenic antisite may be produced by

$$As_{As} + (V_{Ga})_2^- = As_{Ga} + V_{Ga}\,V_{As} + e^- \qquad (7.12)$$

From Eq. (7.12) it is noted that the concentration of $(V_{Ga})_2^-$ and As_{Ga} might be proportional to each other. Ozeki [30] has pointed out that the EL2 level

may be due to two levels which are close to each other in energy. Thus, these two levels may in fact be contributed by the $(V_{Ga})_2^-$ and As_{Ga} antisite defect, as discussed above. The capture cross section for the EL2 level is around $5x10^{-13}$ cm^2.

Based on the model described by Zou [29] and Ozeki [30] and the results shown in Fig. 7.12, it is believed that the EL2 level observed in the (211A) oriented VPE GaAs samples may be attributed to the $(V_{Ga})_2$ related defect, while the EL2 level observed in the <211B> oriented VPE GaAs samples may be due to the As_{Ga} antisite defect.

7.2.2 LPE n-GaAs Samples

Four samples of LPE GaAs were prepared for the purpose of studying grown-in defects vs. growth temperature and growth rate in the high purity n-GaAs epilayers. These samples were prepared by infinite solution melt liquid phase epitaxy technique grown at 700°C and 800°C with cooling rates of 1°C/min. and 0.4°C/min., respectively. C-V and DLTS measurements were made on these samples, and the results were analyzed. Fig. 7.13 shows the DLTS thermal scans of electron trap (EB4) for samples grown at 800°C and 700°C with cooling rate of 1°C/min.. Note that for same cooling rate, sample grown at 800°C has defect density six times lower than that of 700°C grown sample. On the other hand for sample grown at 700°C and 800°C with cooling rate of 0.4°C/min., no electron traps were detected in these samples. The results of our DLTS and C-V measurements on the LPE GaAs grown by infinite solution melt liquid phase epitaxial technique were summarized in Table 7.2. As noted in Table 7.2, the background carrier density in these samples was around 10^{16} cm^{-3} (as determined by the C-V measurements).

7.2.3 The LEC p-GaAs Samples

Grown-in deep-level defects in several undoped p-GaAs specimens grown by liquid encapsulated Czochralski technique have been studied by the DLTS and C-V measurements using Schottky barrier structure. The DLTS results revealed that the defect spectra in the LEC p-GaAs samples are quite different from those observed in the VPE and LPE GaAs samples discussed in the previous sections.

Fig. 7.14 shows the DLTS scan of a hole trap with a measured activation energy $E_T = E_v+0.134$ eV. If the temperature dependence of the hole capture cross section (i.e., $\sigma_p = \sigma_\infty \exp(-\Delta E_b/kT)$) is taking into account (i.e., $\Delta E_b = 0.054$ eV), then the actual activation energy for this hole trap should be around 80 meV (i.e., $E_v+0.08$ eV) as shown in Fig. 7.15. This value is in excellent agreement with the value obtained from Hall effect and photoluminescence measurements. This hole trap is a double charged acceptor center and is due to the gallium antisite defect, Ga_{As}. The density of this hole trap is quite high (N_T varies from mid 10^{15} cm^{-3} to mid 10^{16} cm^{-3}). It was observed for the first time in the LEC p-GaAs specimens by the DLTS technique. In addition to the hole trap observed in these p-GaAs samples, we also observed an electron trap with activation energy at $E_c-0.12$ eV and $E_c-0.18$ eV; this is shown in Fig. 7.16. Table 7.3 summarizes the defect parameters deduced from the DLTS and C-V data for several LEC grown p-GaAs samples.

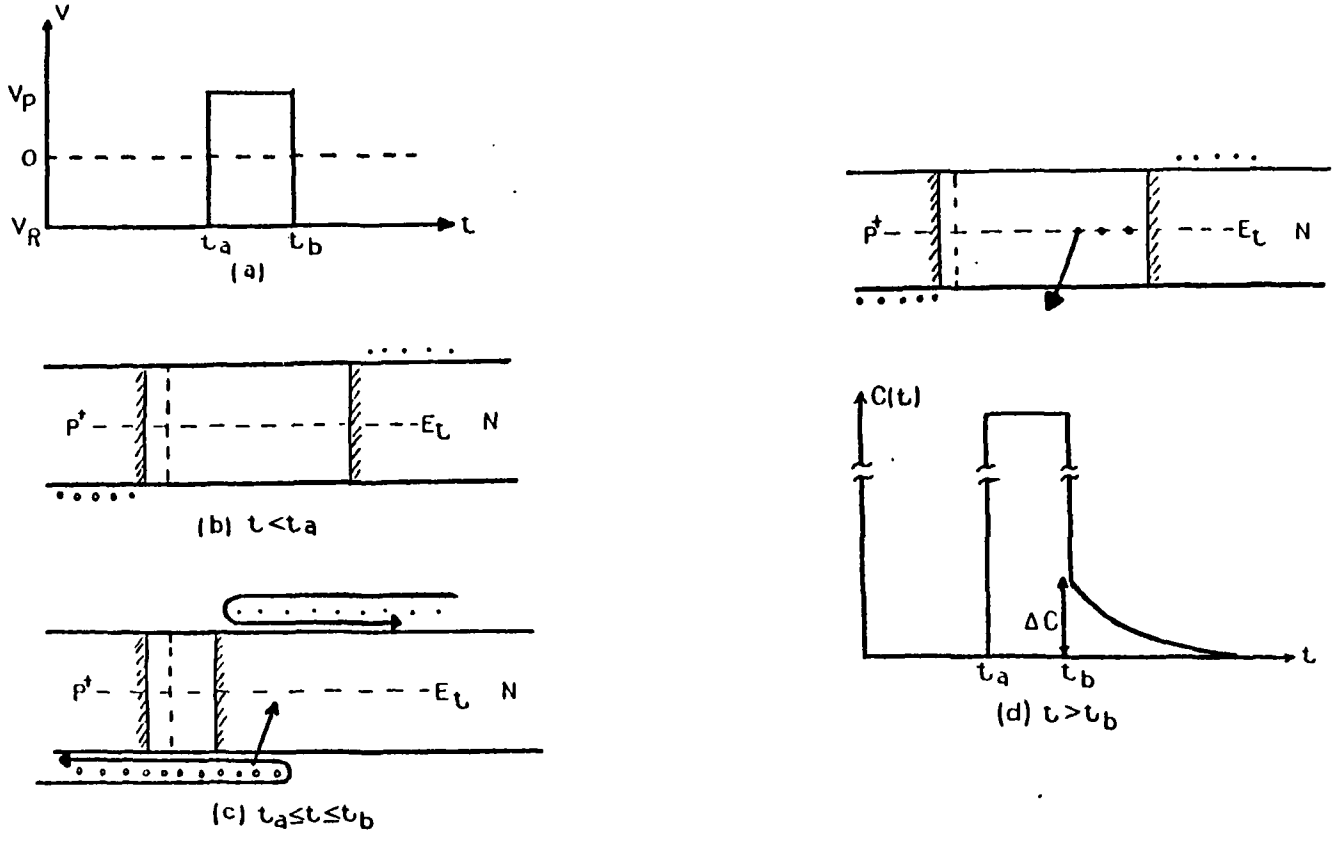

Fig. 7.1 Schematic diagrams of minority carrier injection process in a p-n diode in the DLTS measurement.

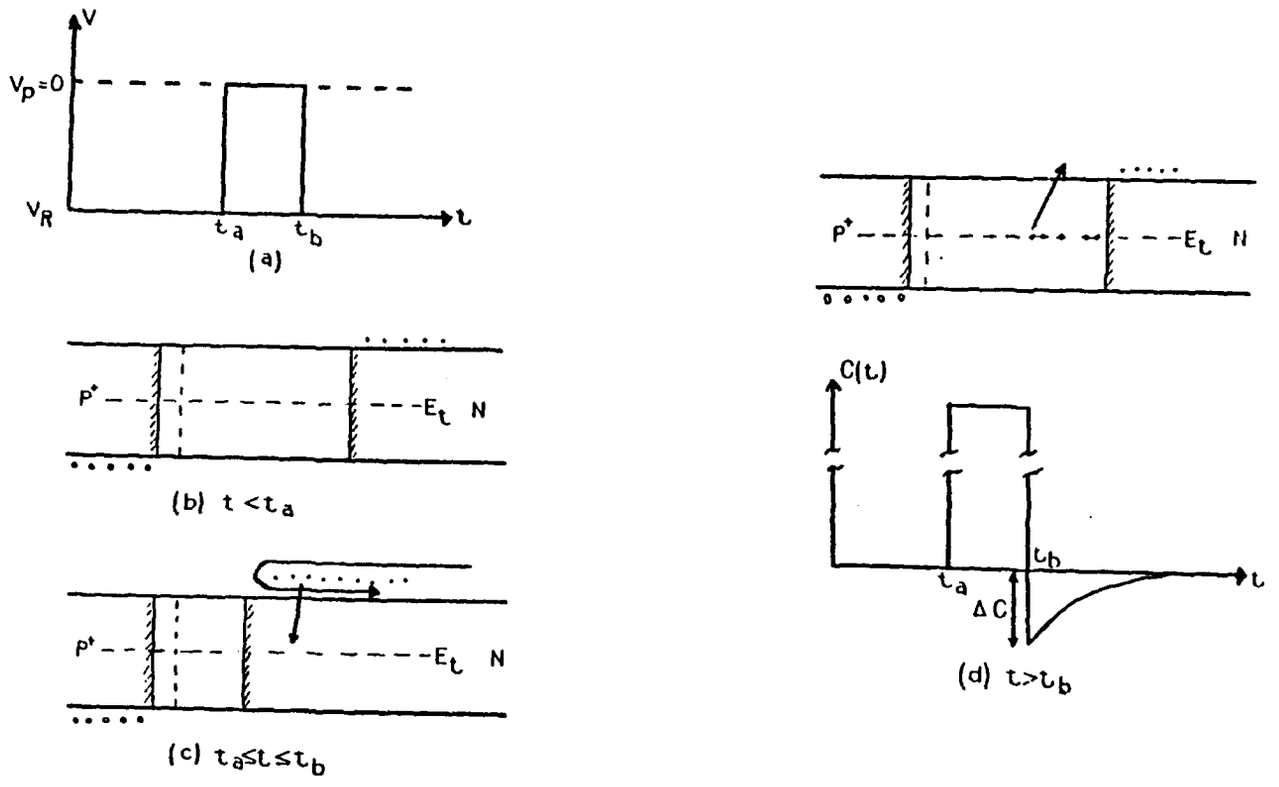

Fig. 7.2 Schematics of majority carrier injection process in a p-n diode in the DLTS measurement.

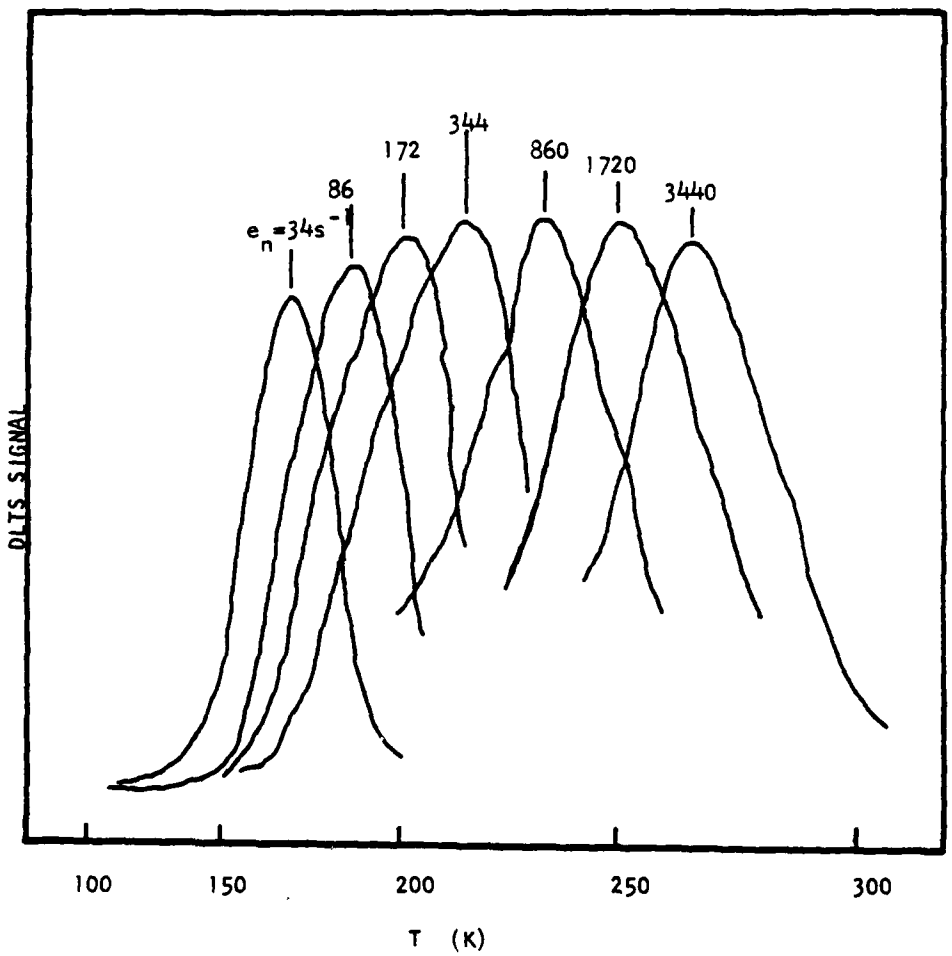

Fig. 7.3 Peaks of DLTS signals shifting as a function of emission rate.

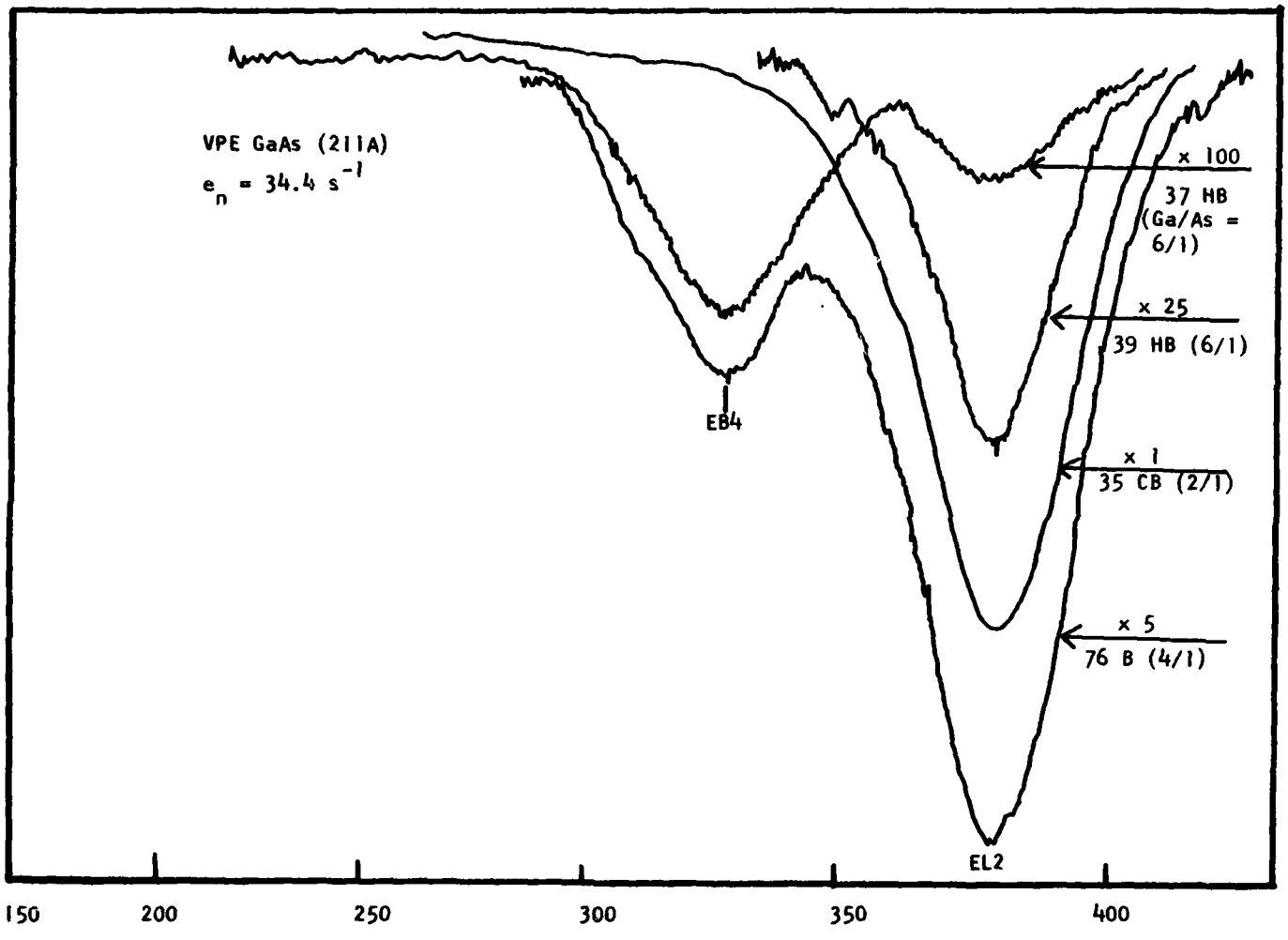

Fig. 7.4 DLTS scans of electron traps for VPE GaAs samples grown on (211A) oriented substrates with Ga/As ratio changing from 2/1 to 6/1.

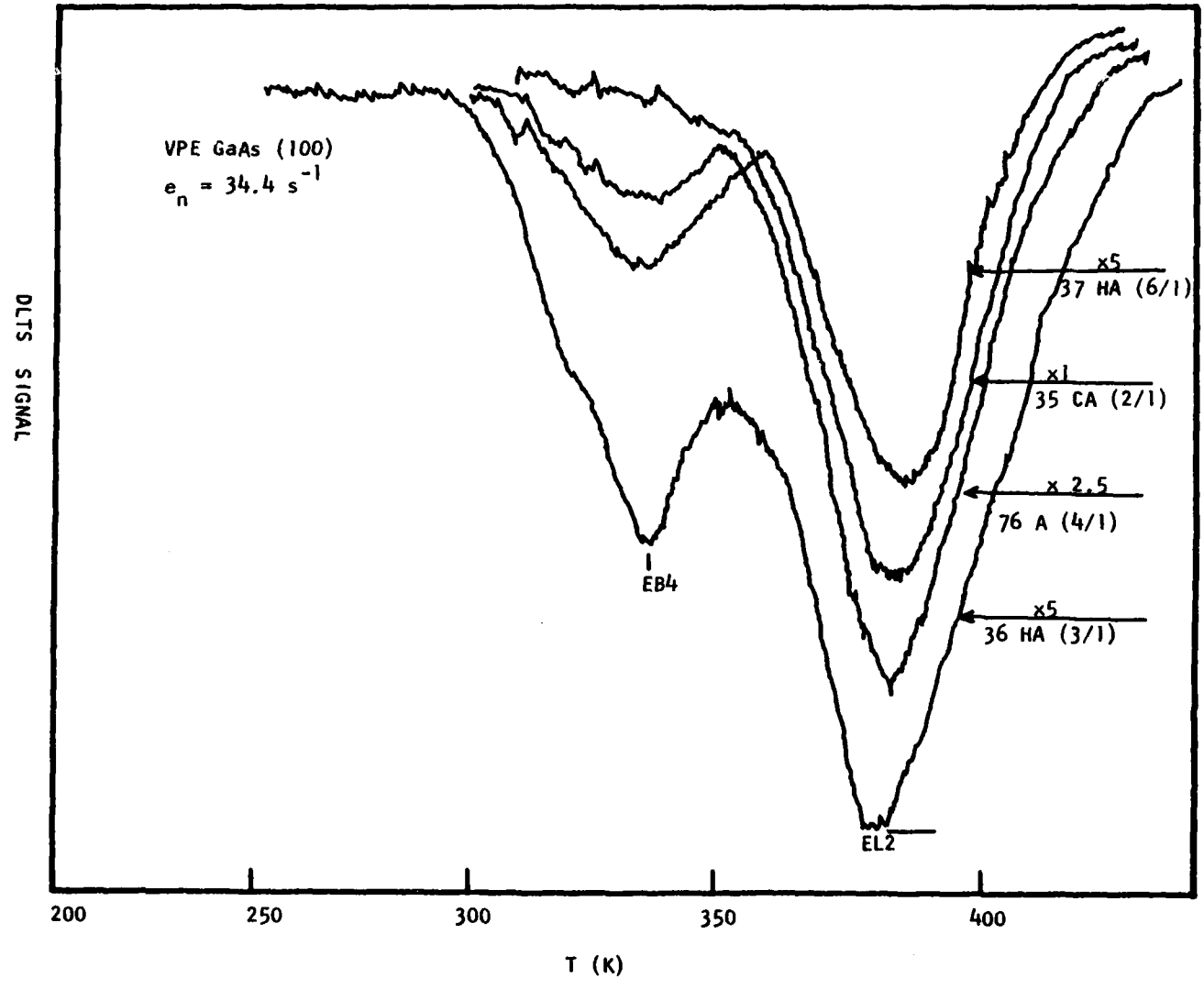

Fig. 7.5 DLTS scans of electron traps for VPE GaAs samples grown on (100) oriented substrates with Ga/As ratio varying from 2/1 to 6/1.

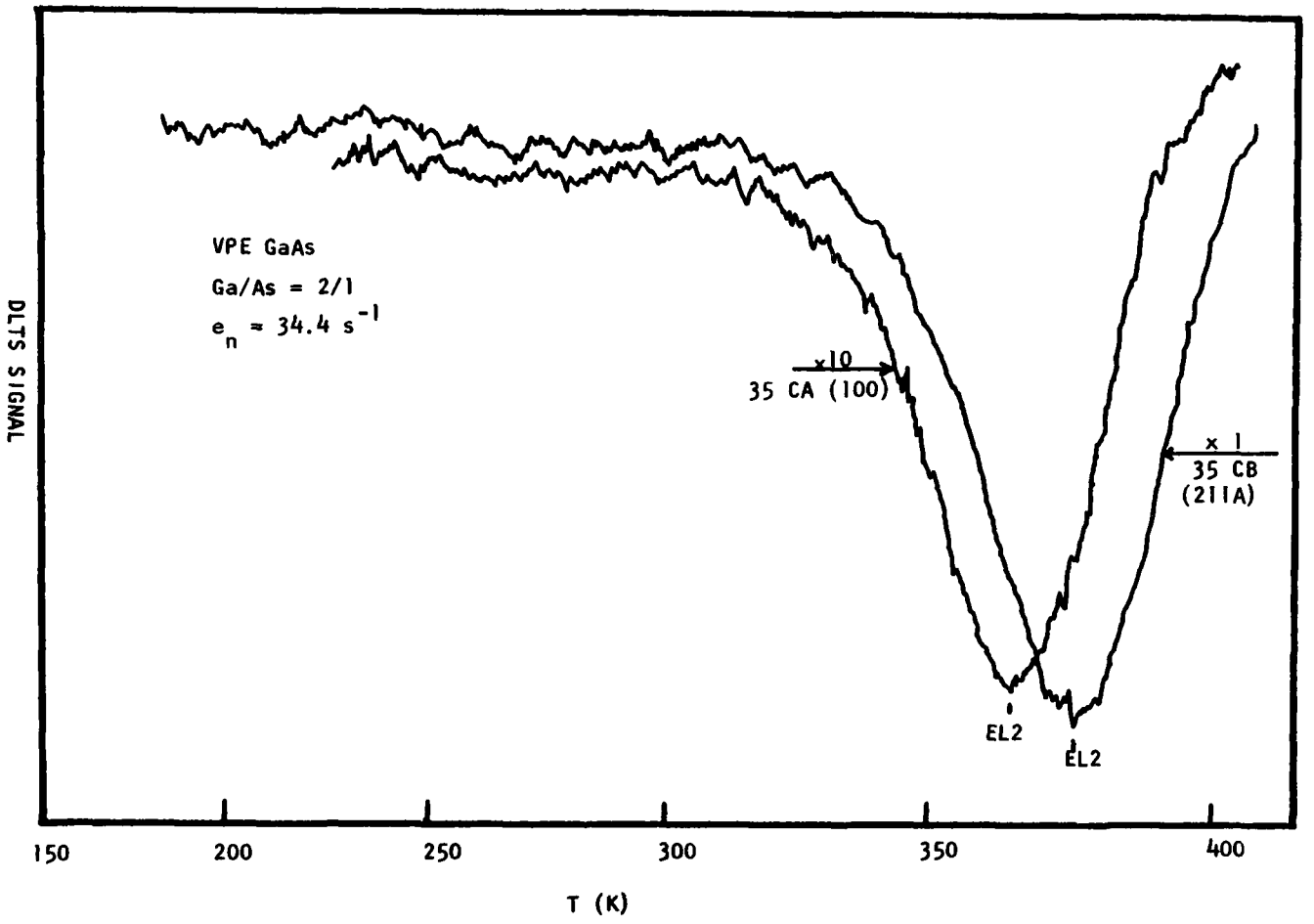

Fig. 7.6 DLTS scans of electron traps for VPE GaAs samples grown on (100) and (211A) substrates with Ga/As ratio = 2/1. Both samples were grown under identical conditions.

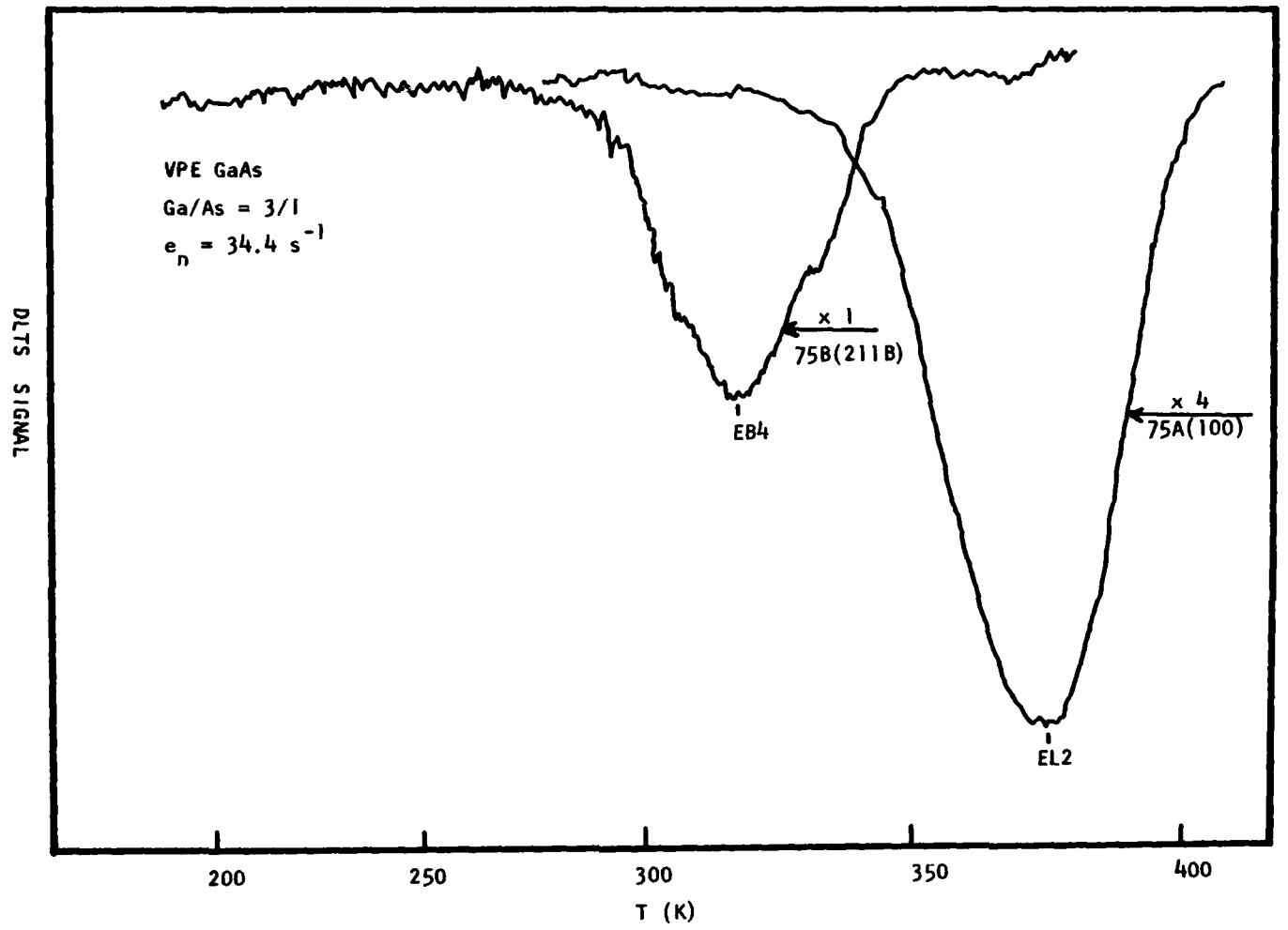

Fig. 7.7 DLTS scans of electron traps for two VPE samples with (100) and (211B) orientations.

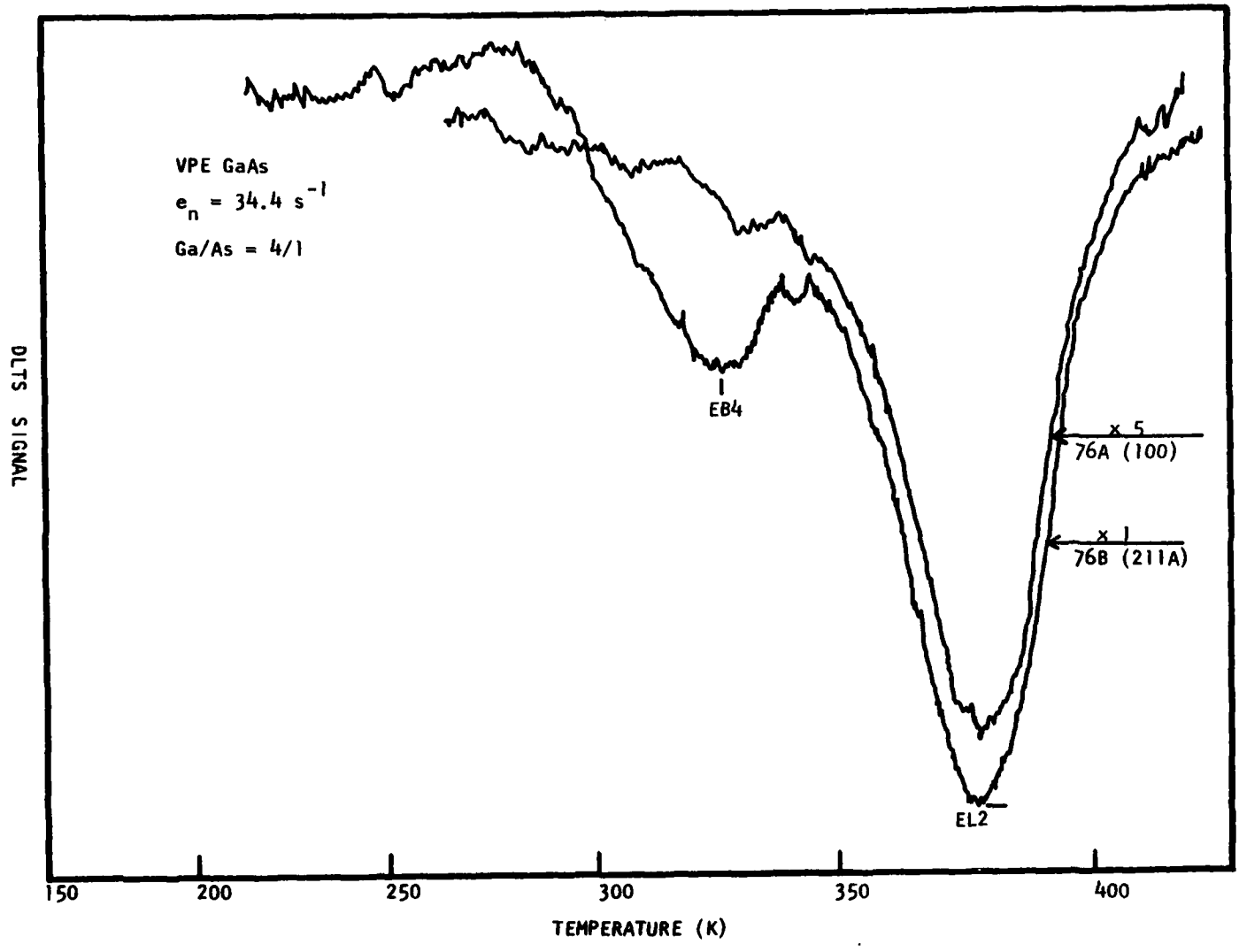

Fig. 7.8 DLTS scans of electron traps for two VPE samples with(100) and (211A) orientations and Ga/As ratio equal to 4/1.

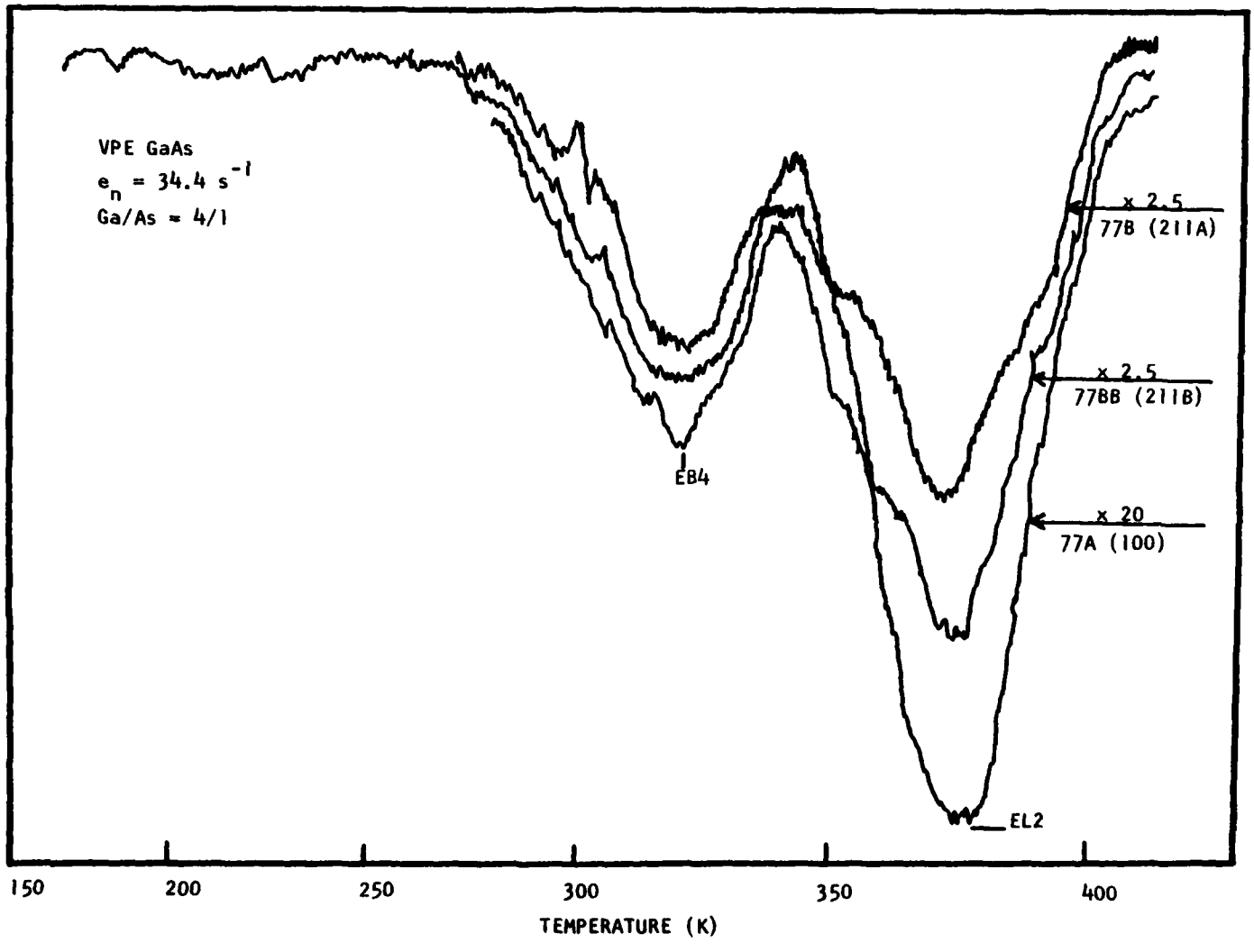

Fig. 7.9 DLTS scans of electron traps for VPE GaAs samples grown on (100),(211A) and (211B) oriented substrates with Ga/As ratio equal to 4/1.

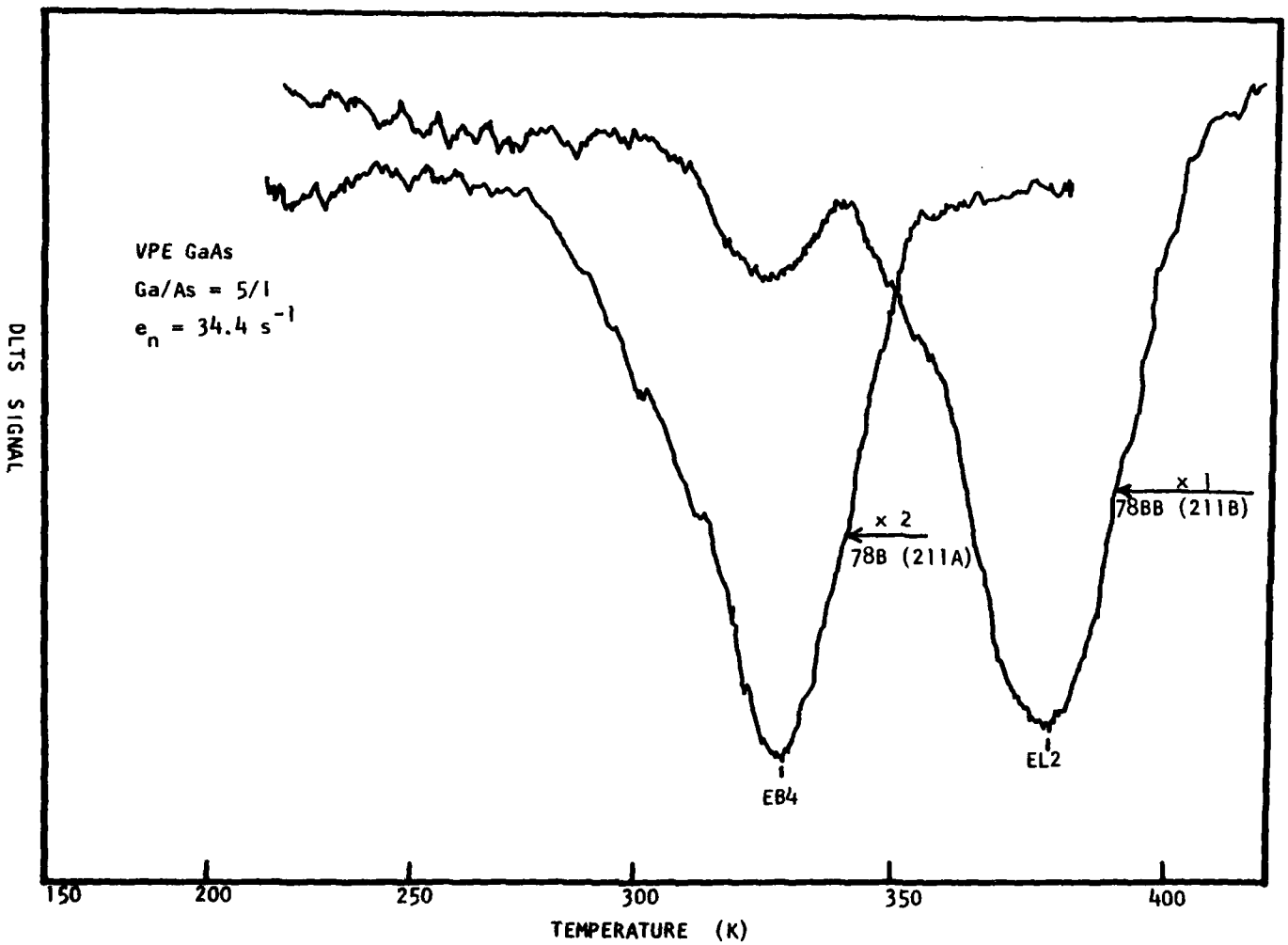

Fig. 7.10 DLTS scans of electron traps for the VPE GaAs samples grown on (211A) and (211B) oriented substrates with Ga/As ratio = 5/1.

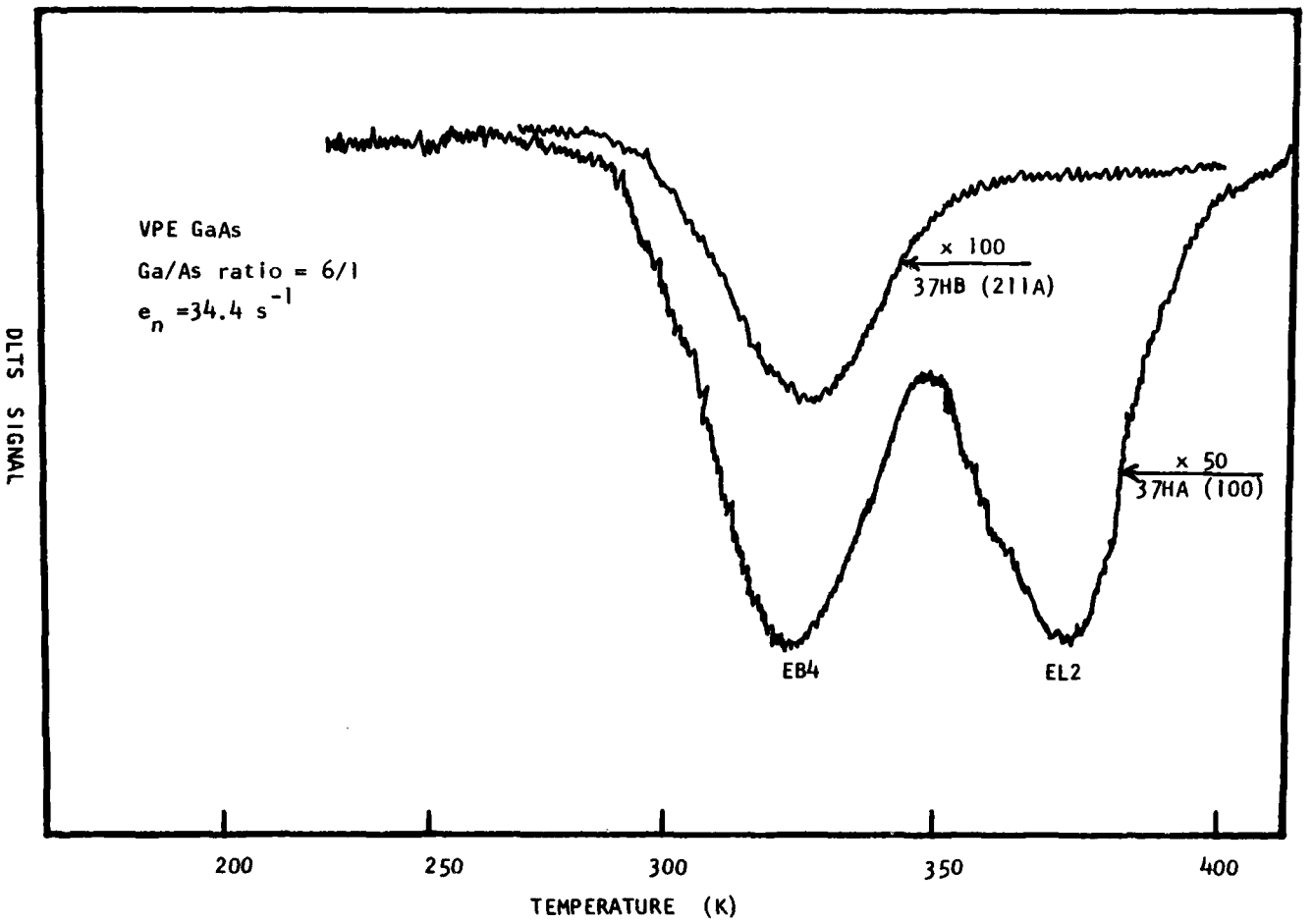

Fig. 7.11 DLTS scans of electron traps in the VPE GaAs samples grown on (100) and (211A) oriented substrates with Ga/As ratio = 6/1.

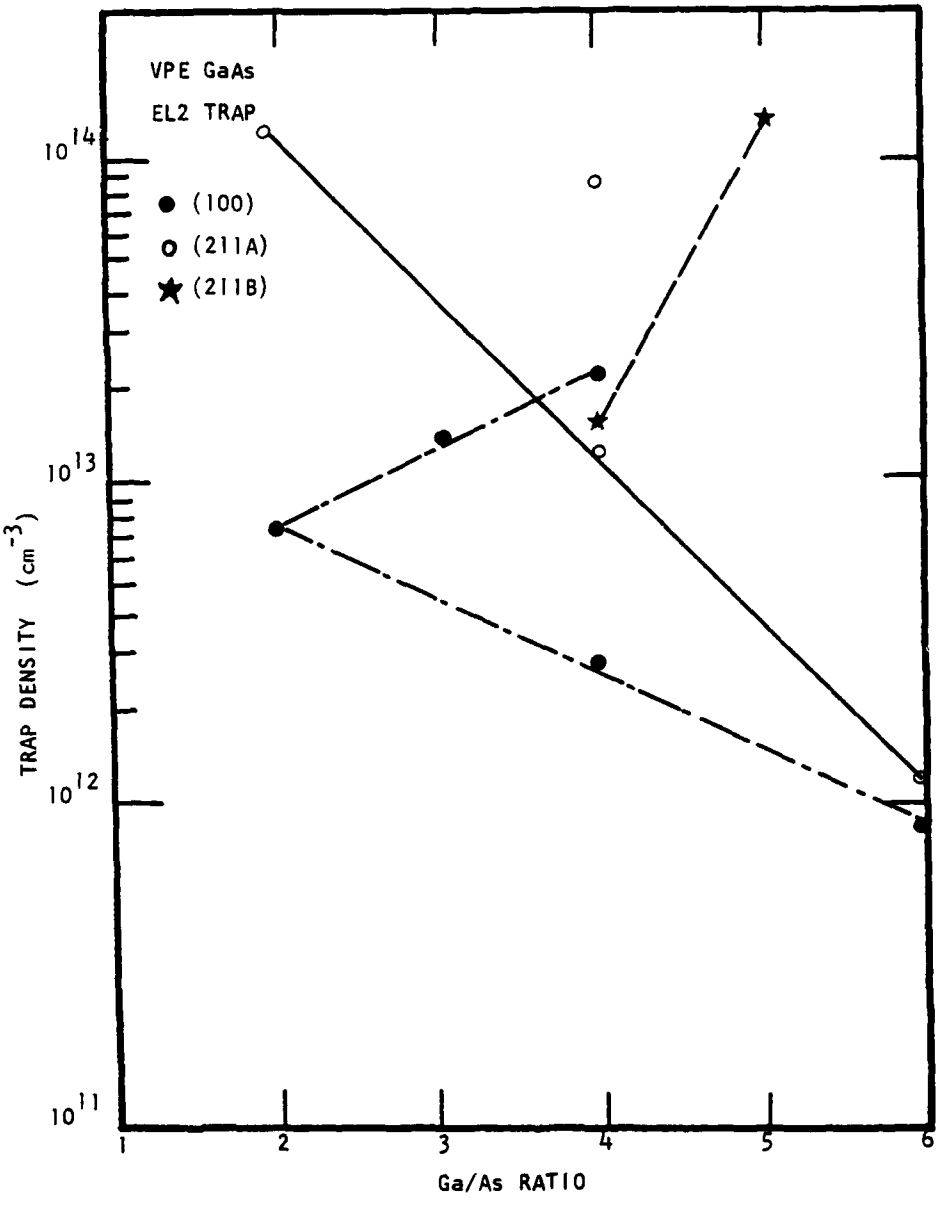

Fig. 7.12 Density of EL2 level vs Ga/As ratio in VPE GaAs samples Grown on (211A),(211B),and(100) oriented substrates.

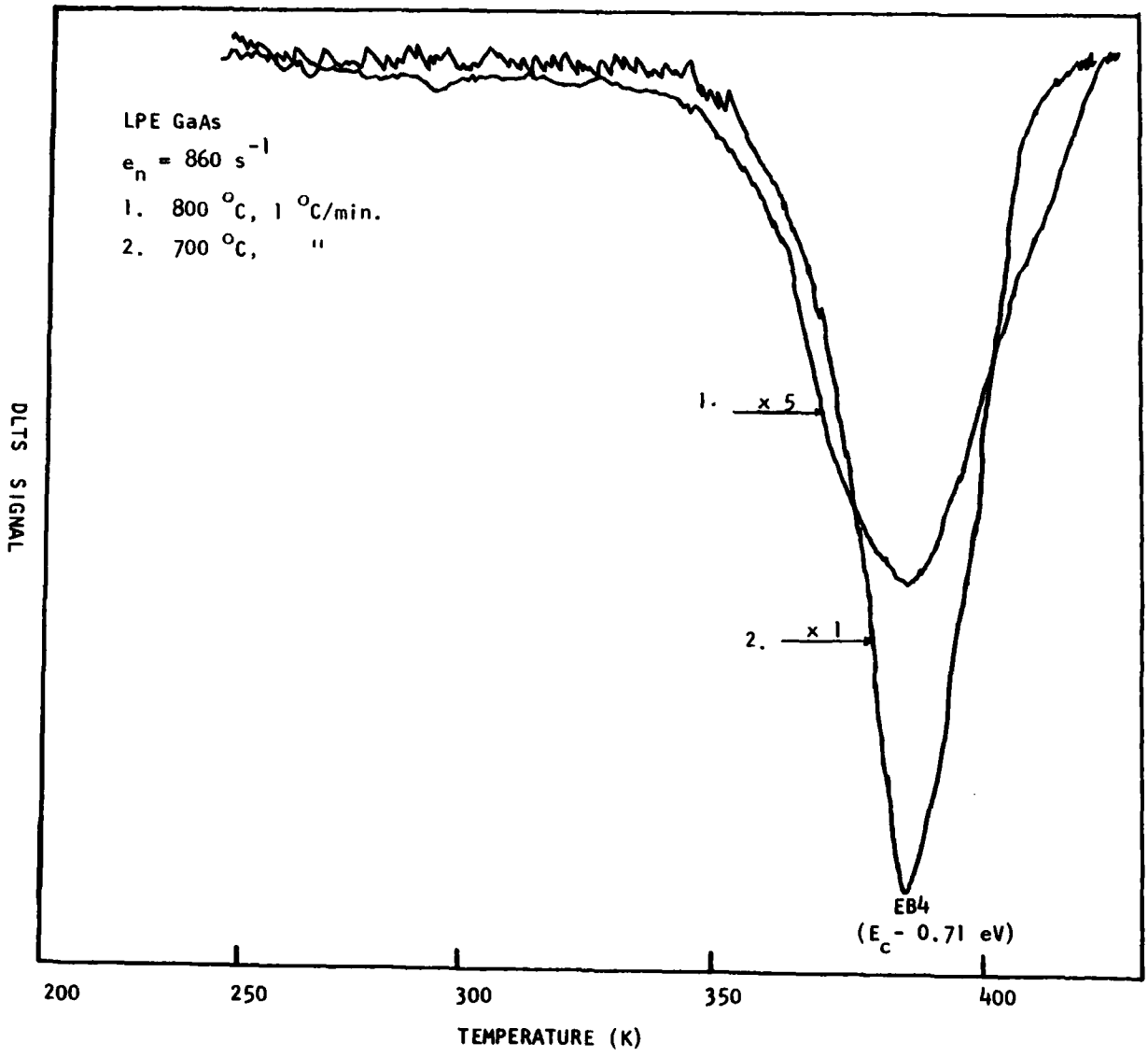

Fig. 7.13 DLTS scans of electron trap for two LPE GaAs samples grown at 700 and 800 °C with 1 °C/min. cooling rate.

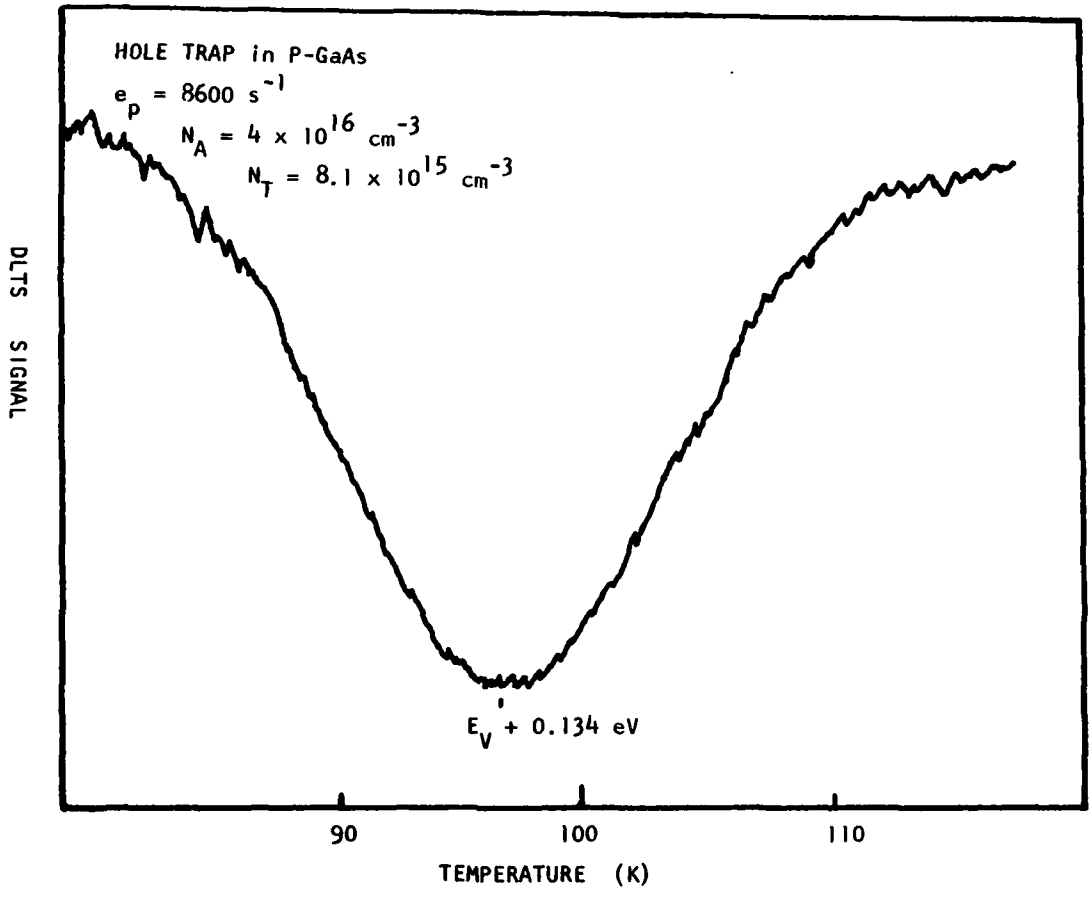

Fig. 7.14 DLTS scan of hole trap in p-GaAs grown by liquid encapsulated Czochralski (LEC) technique. The hole trap is attributed to the Ga_{As} antisite defect (*double acceptor state*).

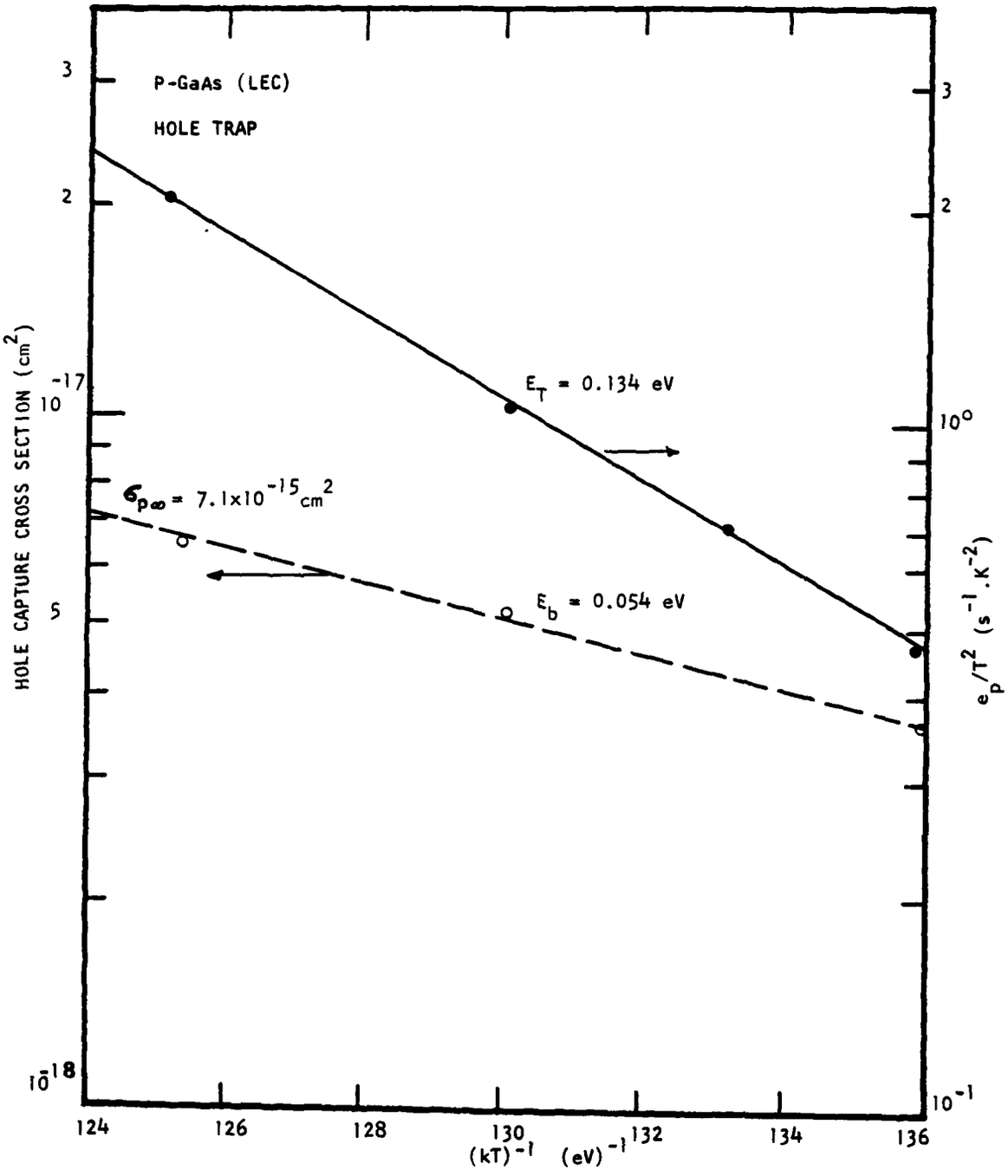

Fig. 7.15 The temperature dependence of hole emission rate and capture cross section of the hole trap observed in LEC p-GaAs sample.

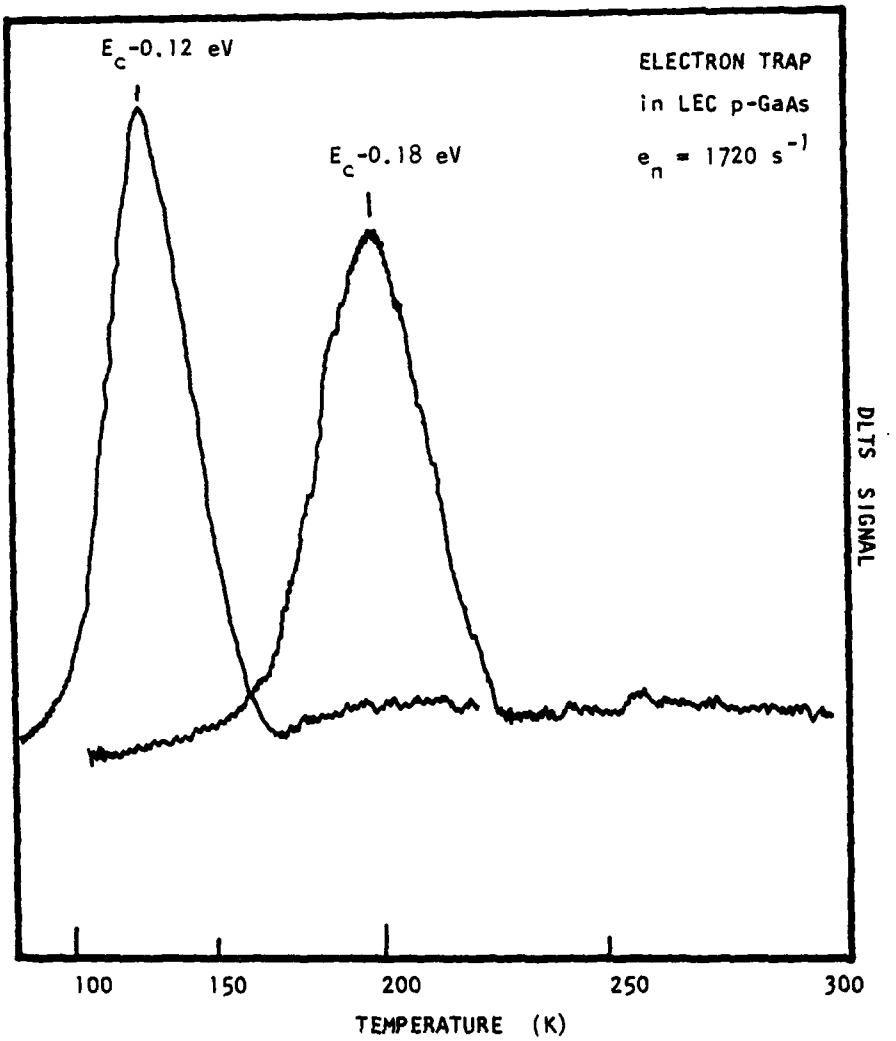

Fig. 7.16 DLTS scans of electron traps in LEC p-GaAs samples.

Table 7.1 Electron trap parameters vs. growth parameters in VPE GaAs

Sample No.	Orientation	N_D (cm^{-3})	Electron Traps				Ga/As ratio	Growth temp. (°C)
			E_T (eV)	N_T (cm^{-3})	E_T (eV)	N_T (cm^{-3})		
35 CA	100	6.7×10^{14}	EB4 = $E_c-0.71$	-	EL2 = $E_c-0.83$	7.6×10^{12}	2/1	715
35 CB	211A	1.7×10^{15}	"	-	"	1.2×10^{14}	2/1	715
75 A	100	7.2×10^{14}	"	-	"	1.5×10^{13}	3/1	725
75 B	211 B	3×10^{15}	"	3.9×10^{13}	"	-	3/1	725
76 A	100	3×10^{15}	"	2×10^{12}	"	2.2×10^{13}	4/1	725
76 B	211A	5.5×10^{15}	"	3×10^{13}	"	9×10^{13}	4/1	725
77 A	100	1×10^{15}	"	8×10^{11}	"	2.6×10^{12}	4/1	750
77 B	211A	7.2×10^{15}	"	1×10^{13}	"	1.2×10^{13}	4/1	750
77 BB	211B	5.6×10^{15}	"	1×10^{13}	"	1.6×10^{13}	4/1	750
78 B	211A	3.7×10^{15}	"	4.3×10^{13}	"	-	5/1	725
78 BB	211B	1×10^{16}	"	2.9×10^{13}	"	1.4×10^{14}	5/1	725
37 HA	100	1.3×10^{15}	"	1×10^{12}	"	8.6×10^{11}	6/1	725
37 HB	211A	3.1×10^{15}	"	2.4×10^{11}	"	-	6/1	725
39 HB	211A	7.2×10^{14}	"	-	"	1.2×10^{12}	6/1	720

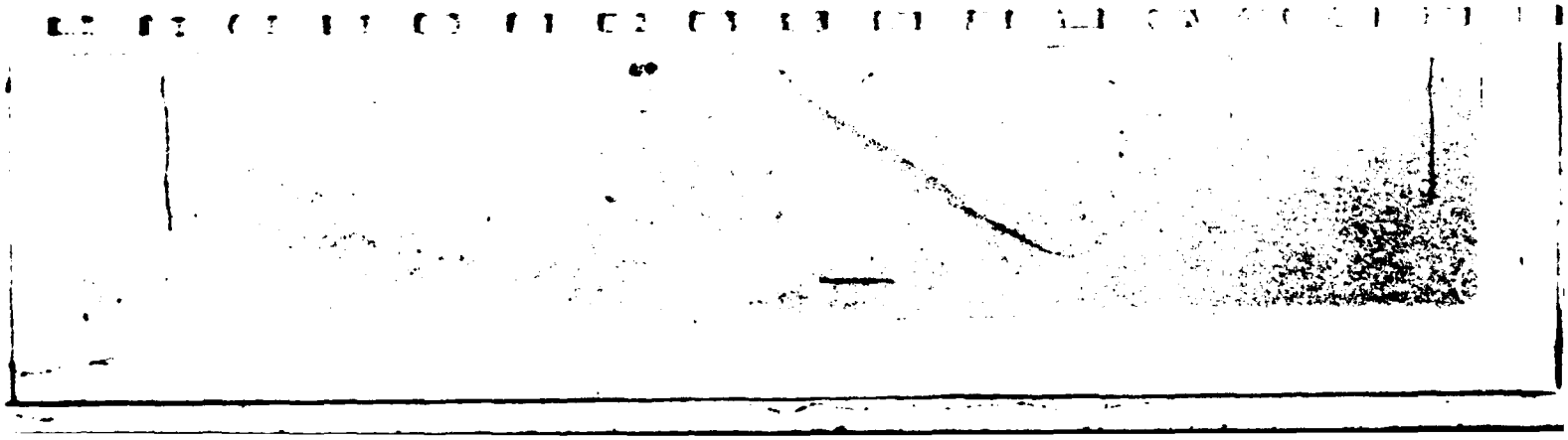

Table 7.2 Grown-In Deep-Level Defects in LPE GaAs* (Hughes' samples)

Sample No.	Growth Temperature and cooling rate	Electron Trap Level (eV)	N_{TT} (cm^{-3})	N_D^+ (cm^{-3})	EPI layer thickness (μm)
LEPI-45	700°C, 0.4°C/min.	-	-	$\sim 9 \times 10^{15}$	2
LEPI-46	700°C, 1°C/min.	E_c-0.71	10^{14}	1.6×10^{16}	3
LEPI-43	800°C, 0.4°C/min.	-	-	$\sim 10^{16}$	5
LEPI-44	800°C, 1°C/min.	E_c-0.71	1.6×10^{13}	2×10^{16}	7.5

*Grown by infinite solution melt liquid phase epitaxial technique at Hughes Research Laboratories.
†Determined from C-V method.

Table 7.3 Defect Parameters in the LEC grown p-GaAs samples

Samples	N_A (cm^{-3})		Electron Trap		Hole Trap	
	77 K	300 K	E_T (eV)	N_T (cm^{-3})	E_T (eV)	N_T (cm^{-3})
#1-3	2.8×10^{17}	4.1×10^{17}	E_c-0.12	$1.\times10^{16}$	E_v+0.134	6.7×10^{16}
#2-1	4×10^{16}	4.4×10^{16}	E_c-0.18	1.6×10^{15}	"	8×10^{15}
#2-2	3.8×10^{16}	4×10^{16}	E_c-0.18	1.3×10^{15}	"	5.8×10^{15}
#2-10	5×10^{16}	6.7×10^{16}	E_c-0.18	-	"	1.4×10^{16}

VIII. THERMAL AND RECOMBINATION ENHANCEMENT (R-E) ANNEALING IN GaAs

There are three thermal annealing stages in gallium arsenide [34]. The first two thermal annealing stages in GaAs occured at 235 K and 280 K, which has been studied in some details by Thommen [35]. Annealing properties in this temperature range have also been observed by Stein [36], Jeong et al [37,38], and Kalma [39]. The third stage occured in the vicinity of 500 K, which have been observed by researchers studying the annealing behavior in the irradiated GaAs. The kinetics of this stage have been studied by Aukerman and Graft [40]. Recombination-enhanced annealing was first studied by Lang and Kimerling [41] in one-MeV electron irradiated GaAs. Weeks et al [42] analyzed the thermodynamics of recombination enhancement annealing and showed, using unimolecular reaction rate theory, that the thermal annealing activation energy of a defect is reduced by an amount less than or equal to the energy released during carrier capture by the defect, provided that the electronic energy can be transferred into the lattice vibration mode which drives the defect motion. During annealing process, defect receives energy created by thermal vibration or recombination process, enabling it to move back to its original lattice site.

8.1 Annealing Mechanism

Consider a defect which has an electronic trap level lying deep in the band gap of a semiconductor, with energy ΔE_c below the conduction band. The electron will be confined to a small region of space in the vicinity of the defect. In addition, because of the difference in mass or coupling to the rest of the lattice, there will be several localized vibrational modes associated with

the defect. In order to be captured by the defect, an electron must lose energy ΔE_c to go from its "free" conduction band state to a bound state localized around the defect. Localized vibrational modes are characterized by large vibrational amplitudes of atoms in the vicinity of the defect. These vibrations are strongly affected by differences in local binding between the free and trapped electronic configurations. A small fraction of the energy ΔE_c may be converted into delocalized lattice vibrations, particularly if trapping occurs by a cascade mechanism. Thus, almost all the energy which is initially deposited into the localized modes of the defect molecule, will eventually flow out to the rest of the lattice as thermal equilibrium is re-established. However, before this occurs, it may be used to promote defect reaction such as diffusion. The number of defects are normally affected by two annealing processes, namely, the thermal annealing and the recombination-enhancement annealing processes. We shall briefly consider the thermal and the recombination-enhanced annealing mechanisms here to aid our explanation of the annealing behavior observed in the VPE GaAs samples. For the thermal annealing process, the annealing rate is in general an exponential function of the temperature, and can be expressed by:

$$K_a(\text{thermal}) = K_t \exp(-E^*/kT) \tag{8.1}$$

where K_t is a proportionality constant, and E^* is the thermal activation energy for the defect annealing.

When recombination-enhancement (R-E) annealing process is added to the thermal annealing process, the annealing rate due to the R-E process is given by:

$$K_a(\text{R-E}) = K_e \exp(-E_e/kT) \tag{8.2}$$

where $$E_e = E_R + E^* - \Delta E \tag{8.3}$$

K_e is a proportionality constant.

In Eq. (8.2), E_e is the recombination-enhanced activation energy. E* is the thermal activation energy defined by Eq. (8.1). E_R is the electron-hole pair recombination activation energy. $\Delta E = E_g - E_t$ is the minority carrier capture energy (E_g is the bandgap energy; E_t is trap energy level). From Eq. (8.3), it is noted that the R-E activation energy is lower than the thermal annealing activation energy E*. Thus, it is obvious that the electron-hole pair capture process can be used to promote annealing reaction and to reduce the annealing activation energy.

From the above discussion, it is clear that the recombination-enhancement annealing process will be most useful and effective if the defects to be annealed are the recombination centers in which capture of electron-hole pair is possible.

8.2 Thermal and Recombination-Enhancement Annealing Experiment in VPE GaAs

Low temperature (200 to 230°C) thermal annealing and recombination-enhancement annealing (by forward bias injection) experiment was performed on one VPE GaAs sample with Ga/As ratio = 2. In this sample, two electron traps (EB4 and EL2) with energies of E_c-0.71 eV and E_c-0.83 eV were observed. The DLTS scans for each of these two electron traps were shown respectively in Fig. 8.1 and Fig. 8.2, under various annealing conditions. Fig. 8.1 shows the EL2 electron trap (E_c-0.83 eV) before and after combined thermal (200°C, 20 and 100 mins.) and recombination enhancement (R-E) annealing. The results showed that the reduction in the density of EL2 is small after annealing. The reason for this may be due to the fact that EL2 level is very deep and is not an effective recombination center , and the thermal annealing activation energy is quite large. Unless higher annealing temperature and higher

injection current are applied to the sample, it is unlikely to see a significant reduction in the density of EL2 level in this VPE GaAs by the combined annealing process. To validate our argument we performed an annealing study on the EB4 level. The annealing temperature was increased to 230°C and the forward bias increased to 1 and 2V. The DLTS results are displayed in Fig. 9.2. The EB4 electron trap is a midgap (E_c-0.71 eV) level which is an effective recombination center. Thus, combined thermal and recombination enhancement annealing process should be more effective in this case for reducing the density of the EB4 level. This is indeed the case, as is clearly illustrated in Fig. 8.2. The density of EB4 level was reduced substantially followed by a 2 hour 230°C thermal annealing and by applying a forward bias injection (R-E) annealing. Additional studies of the annealing behavior in the VPE, LPE, and LEC grown GaAs samples are currently being undertaken, and the results will be reported later.

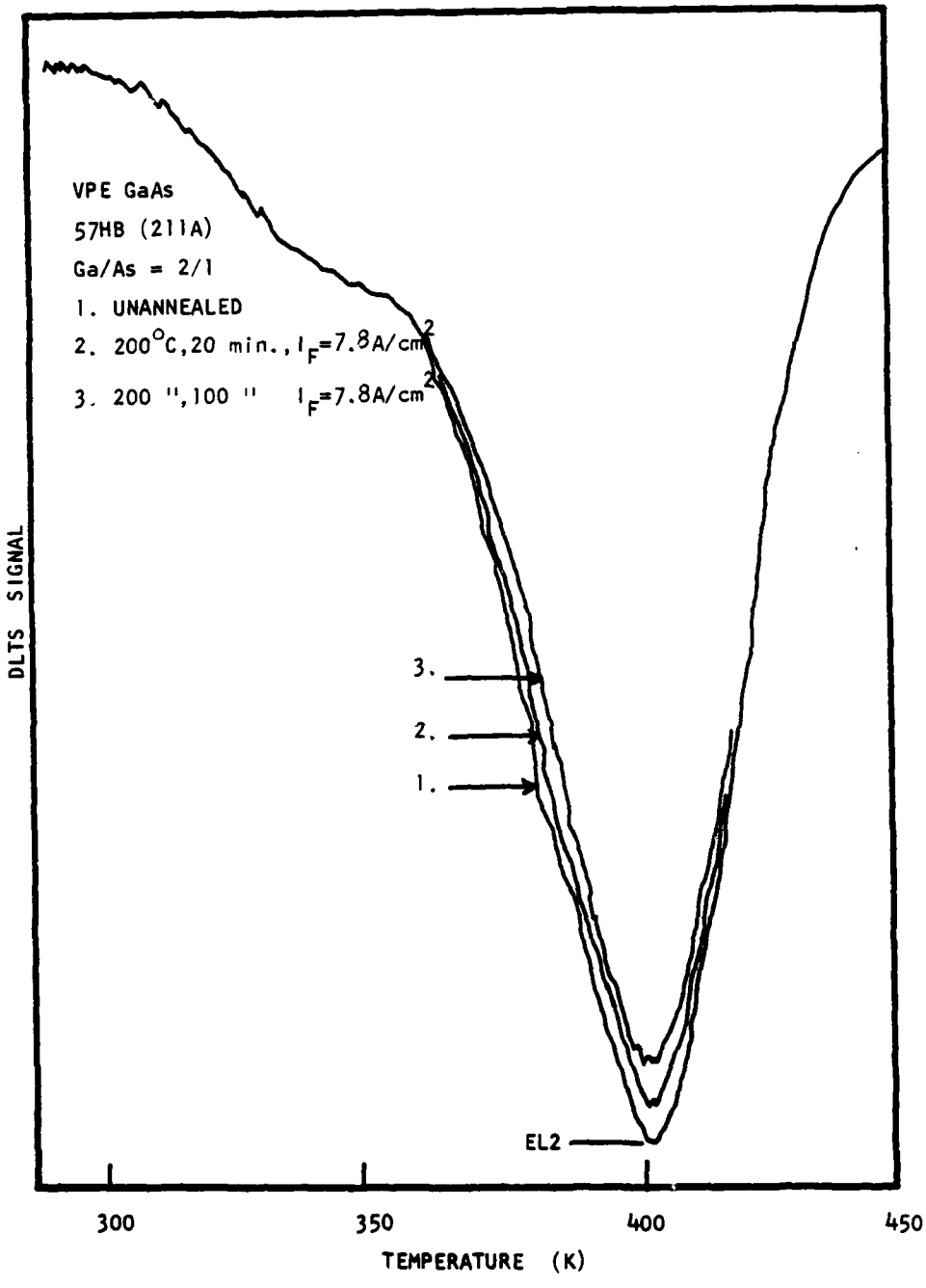

Fig. 8.1 DLTS scans of EL2 level as a function of combined thermal and recombination-enhanced annealing condition.

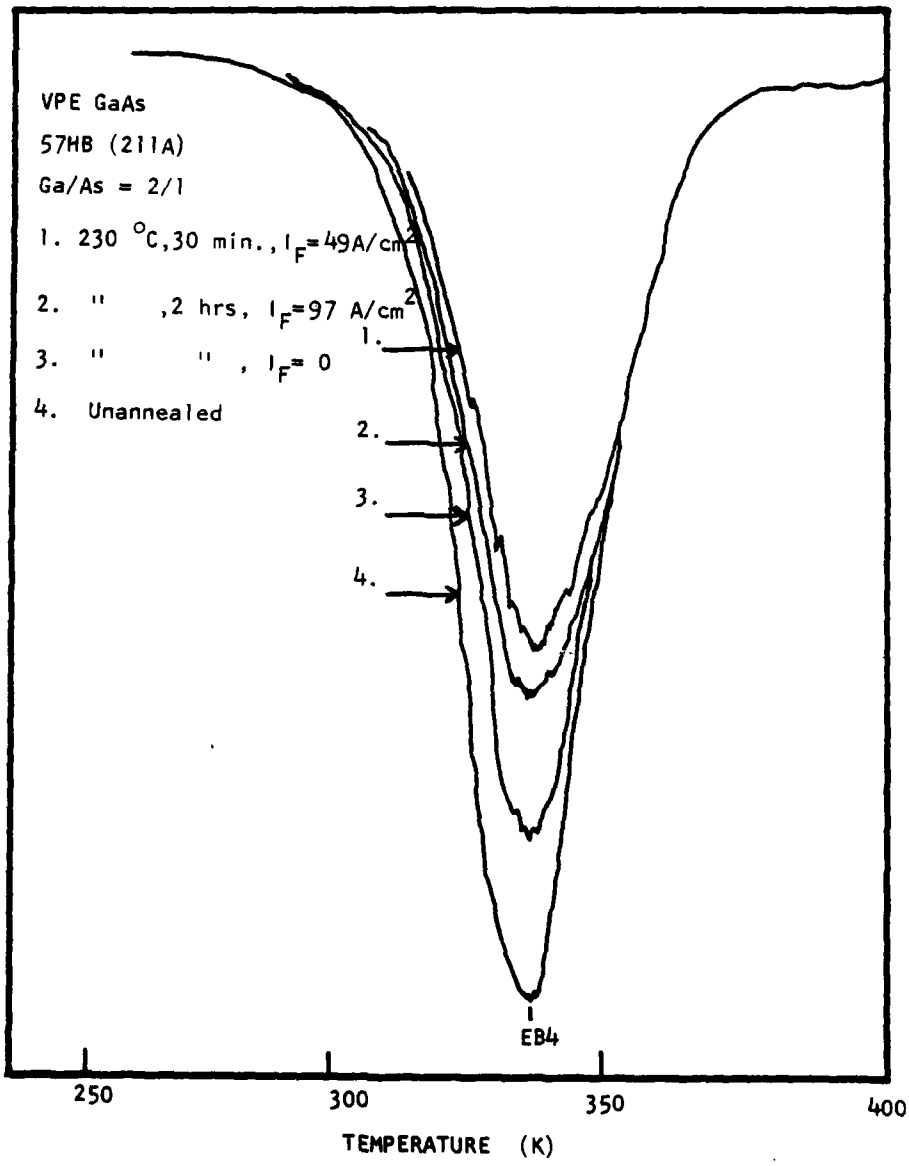

Fig. 8.2 DLTS scan of EB4 electron trap vs different annealing conditions(combined thermal and injection annealing).

IX. SUMMARY AND CONCLUSIONS

Studies of grown-in deep level defects and transport parameters in gallium arsenide grown by VPE, LPE, and LEC techniques under various growth conditions have been carried out in this work. The main technical finding and conclusions are listed as follows:

(i) VPE GaAs Samples Grown by a Novel $Ga/AsCl_3/H_2$ Reactor System:

Study of the grown-in deep level defects in n-type VPE GaAs samples vs. substrate orientations, Ga/As ratios (2/1 to 6/1), and growth temperature (715 to 750°C) has shown that one to two electron traps (i.e., EB4 = E_c-0.71 eV, and EL2 = E_c-0.83 eV) exist in these VPE GaAs samples. From the results of our DLTS and C-V analysis, it is found that (1) background carrier concentration are two to five times higher for the <211 > samples than the <100> samples; (2) defect density was in general higher for the <211> samples than the <100> samples, (3) density of EL2 level was found to decrease with increasing Ga/As ratio for the <211A> samples, and increases with Ga/As ratio for the <211B> samples, (4) for the <100> samples, the density of EL2 level may either increase or decrease with Ga/As ratio depending on the types of defects formed during the growth, (5) the EL2 level may be attributed to either antisite defect (As_{Ga}) or gallium-divacancy defect, $(V_{Ga})_2$, (6) the EB4 electron trap may be due to the bound pair of antisite defect, As_{Ga} Ga_{As}, which is a neutral defect, (7) the combined thermal and recombination enhancement annealing process can effectively reduce the density of grown-in defect such as EB4 studied in this report, and (8) increasing growth temperature from 715 to 750°C appears to be beneficial for reducing defect density in the VPE GaAs.

(ii) LPE GaAs Samples Grown by Infinite Solution Melt Technique:

Studies of the grown-in defects and transport properties in four n-type LPE GaAs specimens vs. growth temperature (700°C and 800°C) and temperature drop rate (0.4°C/min. and 1°C/min.) have been made in this work. The results showed that only one electron trap (EB4) with energy of E_c-0.71 eV was observed in samples grown at 700 and 800°C with temperature drop rate of 1°C/min. (none for the 0.4°C/min. drop rate samples). Resistivity and Hall effect measurements showed that sample grown at 700°C with 0.4°C/min. drop rate has the highest electron mobility and lowest carrier concentration at 77 K. Thus, reducing the temperature cooling rate during the epitaxial layer growth appears to be benefical for reducing the density of grown-in defects in the LPE GaAs.

(iii) GaAs Samples Grown by LEC Technique:

Studies of grown-in defects in p-type GaAs specimens grown by liquid encapsulated Czochralski technique have been made using DLTS and C-V methods. The results showed that a new hole acceptor level with energy of E_v+0.080 eV (after correction of temperature dependence factor in the capture cross section) has been observed in the LEC grown p-type GaAs samples; the density of this hole trap is around 10^{16} cm^{-3}, and its origin is believed to be due to the gallium antisite double acceptor center(i.e.Ga_{As})as confirmed by the Hall effect and photoluminescence measurements. An electron trap with energy of E_c-0.18 eV has also been detected by the DLTS measurement. However, the density of this electron trap is significantly lower than that of the hole trap reported above.

(iv) $Al_{0.3}Ga_{0.7}As$ and GaAs LPE Samples:

Studies of the grown-in defects and thermal annealing effects in $Al_{0.3}Ga_{0.7}As$ and GaAs epitaxial layers grown by liquid phase epitaxy technique

have also been carried out in this work, and the results are described in the paper attached in the appendix of this report. It is interesting to note that the defect spectra observed in the $Al_{0.3}Ga_{0.7}As$ LPE samples are totally different from that of GaAs LPE samples, as shown in the appendix.

From the results of our study of the grown-in defects and transport properties in the VPE, LPE, and LEC GaAs samples, it is clear that grown-in defects and background carrier concentration are sensitive to the growth conditions, stoichiometry and substrate orientations. Therefore, a systematic study of the grown-in defects vs. growth parameters in the III-V compound semiconductors should be conducted in order to gain new insight concerning the physical origins of the grown-in defects in these materials.

The future plans for this research program will be to continue our present efforts and to extend our study to include InP and Other III-V ternary compound semiconductors.

X. INTERACTIONS WITH RESEARCHER AT THE GOVERNMENT AND INDUSTRIAL LABS.

In an effort to promote the exchange of research results and to foster cooperation among those currently being supported by AFPSR, Dr. G. L. Witt, the program manager at the AFPSR, has encouraged this principal investigator to interact with researchers at the Air Force Avionic Lab. As a result, Dr. Li was invited in July, 1981, by Dr. P. Stover to give a seminar on the defect characterization in GaAs and other III-V compounds at the Avionic Lab. Subsequently, technical collaboration was established among Drs. Li, Colter, and Litton, in which Dr. Li has agreed to perform defect characterization on the VPE GaAs samples prepared by Dr. P. C. Colter at the Avionic Lab. More than a dozen of the VPE GaAs samples prepared by Dr. Colter have been sent to Dr. Li for characterization, and the data presented in section-1 of this proposal are part of the result of this collaboration. In addition, a joint technical paper has also been prepared and presented at the SPIE technical symposium, held in Los Angeles, on January 25-28, 1982. It is anticipated that this collaboration will be continued in the second year of this research program in which characterization of III-V compounds grown by the VPE, MBE, and MOCVD techniques will be made by Dr. Li in the second year program. Technical collaboration between Dr. Li and R. Loo of Hughes Research Lab. has also been fruitful, Dr. Loo has grown high purity GaAs LPE layers by using infinite solution melt technique for Dr. Li to study grown-in defects in these samples. Some of the data presented in section 1 of this research proposal are the results of this collaboration. In addition, Dr. S. Bedair of the Research Triangle Institute, has also prepared several Al Ga As samples by using the LPE technique for Dr. Li to study the grown-in

defects in the III-V ternary compounds. The results of this study have been published or presented at the conferences [3-4].

Initial contact with Dr. John Kennedy at Rome Air Development Center has been made to discuss possible collaboration on characterization of defect and transport properties in the InP material. Dr. K. Vaidyanathan of Hughes Research Lab. has also expressed interests in establishing a technical collaboration with this principal investigator to work on defect characterization in InP materials. Some p-type InP Schottky diodes made by Hughes Research Lab. has been received by Dr. Li for defect study.

In addition to the interactions cited above, Dr. Li has also been working closely with Dr. P. W. Yu at the Air Force Avionic Lab., on p-type GaAs material grown by the liquid encapsulation (LEC) technique. This joint research effort has been focussed on the characterization of a new acceptor level (hole trap with energy equal to 80 meV) discovered recently in the LEC grown p-GaAs material by the DLTS photoluminescence and Hall effect measurements.

Dr. Li will also be working closely with Dr. Tim Anderson at the Department of Chemical Engineering of the University of Florida, who is currently setting up an LPE growth facility for growing the InP and InGaAs P compound semiconductors. His program is supported by Dr. John Kennedy of Rome Air Development Center. Dr. Li will study the defect and transport properties in the samples prepared by Dr. Anderson, starting in September, 1982.

XI. CONFERENCE AND JOURNAL PUBLICATIONS

During the first year of this research program, several papers have been prepared for presentation at the research conferences as well as for the journal publications. These are listed as follows:

1. S. S. Li, W. L. Wang, P. C. Colter, C. W. Litton, D. C. Reynolds, D. C. Look, P. W. Yu, "A Novel Ga/$AsCl_3/H_2$ Reactor for Controlling Stoichiometry in the Growth of Vapor Phase Epitaxy (VPE) GaAs," Proc. of the SPIE Symposium, presented at the Los angeles meeting, Jan., 26-28 (1982).

2. S. S. Li, C. Y. Lin, S. M. Bedair, and J. A. Hutchby, "Study of Grown-in Defects and Effect of Thermal Annealing in $Al_{0.3}Ga_{0.7}As$ and GaAs LPE Layers," J. of Electronic Materials, vol. 11, pp. 273-287 (1982).

3. S. S. Li, W. L. Wang, P. C. Colter and C. W. Litton, "Studies of Grown-in Deep Level Defects vs. Growth Parameters in the VPE GaAs Layers," to be presented at the Electronic Materials Conf., Fort Collins, CO, June 23-25 (1982). Paper will be published in J. of Electronic Materials.

4. S. S. Li and W. L. Wang, "Studies of the grown-in Defects and Transport parameters vs. Growth conditions in the LPE and VPE GaAs," submitted to the International Meeting on the Relationship Between Epitaxial Growth conditions and the Properties of Semiconductor Epitaxial Layers," Perpignan, France, Aug. 30-Sept. 1 (1982).

5. P. W. Yu, W. C. Mitchel, M. C. Mier, S. S. Li, and W. L. Wang, "Evidence of Intrinsic Double Acceptor in GaAs," Appl. Phys. Lett., submitted (1982).

XII. LIST OF PERSONNEL INVOLVED IN THIS RESEARCH PROGRAM

In addition to the individuals cited in section X., from government and industrial labs., several of Dr. Li's graduate students, W. L. Wang, K. W. Teng, and H. Saban, and his research associate, Dr. D. W. Schoenfeld, have all made significant contribution to this research program. Drs. P. C. Colter, R. Y. Loo, S. M. Bedair, and P. W. Yu are the key contributors from government and industrial labs. to this research project.

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XIV. Appendix

Journal of Electronic Materials, Vol. 11, No. 2, 1982

STUDY OF GROWN-IN DEFECTS AND EFFECT OF THERMAL ANNEALING IN $Al_{0.3}Ga_{0.7}As$ AND GaAs LPE LAYERS

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(Received July 2, 1981)

Studies of the grown-in deep-level defects in the undoped n-$Al_xGa_{1-x}As$ (x = 0.3) and GaAs epitaxial layers prepared by the liquid phase epitaxy (LPE) techniques have been made, using DLTS, I-V and C-V measurements. The effect of 300 °C thermal annealing on the grown-in defects was investigated as a function of annealing time. The results showed that significant reduction in these grown-in defects can be achieved via low temperature thermal annealing process. The main electron and hole traps observed in the $Al_{0.3}Ga_{0.7}As$ LPE layer were due to the E_c-0.31 eV and E_v+0.18 eV level, respectively, while for the GaAs LPE layer, the electron traps were due to the E_c-0.42 and 0.60 eV levels, and the hole traps were due to E_v+0.40 and 0.71 eV levels.

Key words: Deep-level defects, $Al_{0.3}Ga_{0.7}As$, GaAs, DLTS, thermal annealing, LPE layer.

Introduction

$Al_xGa_{1-x}As$/GaAs material system has been used in a variety of applications ranging from the LED's, lasers, and microwave devices to solar cells [1-5]. For example, a cascade p-n junction solar cell structure with open circuit

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voltage exceeding 2 volts has been reported recently using $Al_xGa_{1-x}As$/GaAs material system [1]. The performance of these devices depends greatly on the quality of the $Al_xGa_{1-x}As$/GaAs materials. In an effort to improve the growth of high quality $Al_xGa_{1-x}As$/GaAs epitaxial layers and to understand the fundamental limitation imposed on these materials, we have conducted a study task which aims at understanding the electrical properties of the grown-in defects and their correlation to the performance characteristics of the $Al_xGa_{1-x}As$/GaAs cascade solar cells. To achieve this goal, methods which could lead to the elimination or reduction of the grown-in defects in this material system were explored. Low temperature thermal annealing is one of the methods employed in this study. Several measurement techniques such as DLTS [6-7], C-V, and I-V methods were used to determine the defect energy levels and defect density as well as recombination parameters. The devices used in this study consist of a Be-diffused $Al_{0.3}Ga_{0.7}As$ and GaAs p-n junction diodes as well as the Ge-doped $Al_{0.3}Ga_{0.7}As$ p-n junction diode. Thermal annealing was performed at 300 °C for 2 and 5 hours in both the $Al_{0.3}Ga_{0.7}As$ and the GaAs LPE samples. The results of our study on the effects of a 300 °C thermal annealing on the grown-in deep-level defects in the $Al_{0.3}Ga_{0.7}As$ and GaAs LPE layers will be discussed in this paper. Complete characterization of the defect parameters in the annealed and unannealed $Al_xGa_{1-x}As$ and GaAs LPE layers was carried out in this work.

Experimental Details

Liquid phase epitaxy (LPE) technique was used to fabricate both the abrupt (Ge-doped) and the diffused (Be-doped) $Al_xGa_{1-x}As$ and GaAs p-n junction mesa diodes for the study of DLTS, C-V, and I-V data. Fig. 1 shows four different diode structures fabricated for this study. Fig. 1a is the Be-diffused $Al_{0.3}Ga_{0.7}As$ p-n junction diode structure (Y-015B); Fig. 1b is the Be-diffused p-$Al_{0.9}Ga_{0.7}As$ on n-$Al_{0.3}Ga_{0.7}As$ p-n junction diode (Y-015C); Fig. 1c is the Ge-doped $Al_{0.3}Ga_{0.7}As$ p-n junction diode (L-119D) and Fig. 1d is the Be-diffused p-$Al_{0.3}Ga_{0.7}As$ on n-GaAs p-n junction diode (L-138D). The high band-gap p-$Al_xGa_{1-x}As$ top layer is normally served as a window layer in the solar cell structure, and is much more heavily doped ($\sim 5\times10^{18}$ cm^{-3}) than the undoped n-$Al_{0.3}Ga_{0.7}As$ and n-GaAs LPE layers.

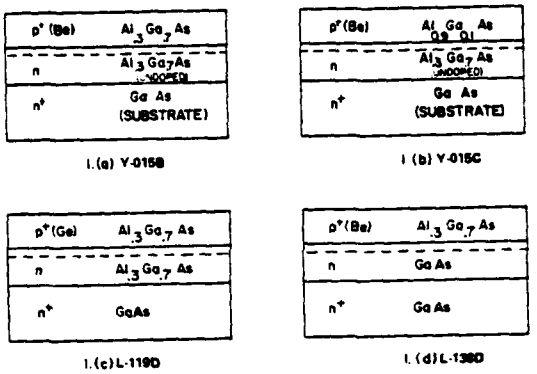

Fig. 1. The junction structures for the Be-diffused and Ge-doped $Al_xGa_{1-x}As$ p-n diodes fabricated by liquid phase epitaxy (LPE) techniques.

Thus, defect characterization by the DLTS method on the device structures shown in Fig. 1 is mainly confined in the undoped n-$Al_{0.3}Ga_{0.7}As$ and n-GaAs LPE layers. However, some influence from the p-$Al_xGa_{1-x}As$ epitaxy layer can be expected in the measurements.

The growth temperature for these samples was held at 800 °C with 1 °C/min. cooling rate. The abrupt junction structure shown in Fig. 1c consists of a Si-doped n-GaAs substrate with $n_o = 2x10^{18}$ cm^{-3} and <111> orientation. Undoped n-$Al_{0.3}Ga_{0.7}As$ and Ge-doped p-$Al_{0.3}Ga_{0.7}As$ epitaxial layers were grown subsequently on this GaAs substrate by the LPE technique. The Be-diffused junction structures shown in Fig. 1a and 1b were identical to the high-bandgap junction used in the cascade solar cells reported previously by Bedair et al. [1]. The Be-doped p-$Al_xGa_{1-x}As$ window layer of 0.2 μm thick was grown on the undoped n-$Al_{0.3}Ga_{0.7}As$ LPE layer. During the process of growing the window layer, "Be" was diffused into the undoped n-$Al_{0.3}Ga_{0.7}As$ and n-GaAs layer to form a diffused p-n junction with junction depth of 0.5 to 1.0 μm. The carrier density in the undoped n-$Al_{0.3}Ga_{0.7}As$ layer was around 10^{16} to 10^{17} cm^{-3}. The Deep-Level Transient Spectroscopy (DLTS) technique [6-7] was employed to identify "grown-in" electron and hole traps in these samples, and the capacitance-voltage (C-V) measurement was

used to determine the background dopant concentration in the undoped n-$Al_{0.3}Ga_{0.7}As$ and n-GaAs LPE layers. The forward I-V measurement was used to determine the dominant current component in these diodes. The results are discussed next.

Results and Discussions

Forward I-V characteristics were first studied to determine the dominant current component (i.e., recombination or diffusion current) in these diodes [4]. For example, if the recombination current in the junction space charge region of the diode dominates the forward I-V characteristics, then

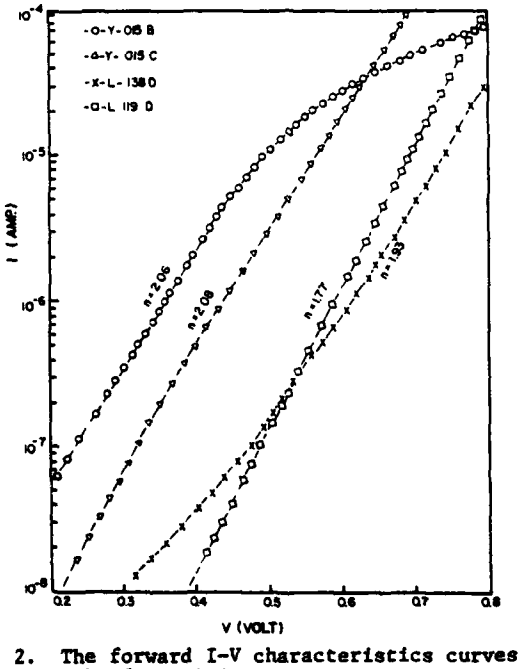

Fig. 2. The forward I-V characteristics curves for the four $Al_xGa_{1-x}As$ p-n junction diodes shown in Fig. 1.

the I-V relation can be described approximately by [4]:

$$I_R \doteq \frac{qn_iWA}{2\tau_o}\exp(-qV/nkT) \qquad (1)$$

where q is the electronic charge; n_i is the intrinsic carrier density; W is the depletion layer width; A is the junction area; τ_o is the effective carrier lifetime in the junction space charge region, and "n" varies between 1 and 2. Fig. 2 illustrates the forward I-V curves for the four different diode structures shown in Fig. 1. The results showed that the Be-diffused $Al_xGa_{1-x}As$ p-n diodes have a much higher dark current values than that of the Ge-doped $Al_xGa_{1-x}As$ p-n diode, while the Be-diffused GaAs p-n diode (L-138D) has the lowest dark current value. In addition, the diode ideality factor "n" was lower for the Ge-doped $Al_{0.3}Ga_{0.7}As$ diode than the Be-diffused diodes. The values of "n" were found to vary between 1.77 and 2.08 for these diodes. This is a clear indication that the recombination current via the deep-level defects in the junction space charge region was the dominant current component in these diodes, and this recombination current component was found closely related to the density of grown-in defects in the junction space charge region of the diodes, as was confirmed by our DLTS data for both unannealed and thermal annealed sample. Fig. 3 shows the forward I-V curves for diode Y-015C ($Al_{0.3}Ga_{0.7}As$) as a function of annealing time. A 300 °C thermal annealing for 2 and 5 hrs. reduces the forward dark current drastically. This result was directly related to the reduction of the grown-in defects in these samples as revealed by the DLTS data to be discussed next. The background dopant density in the undoped n-$Al_{0.3}Ga_{0.7}As$ and n-GaAs LPE layers varies from 2.5×10^{15} to 3×10^{16} cm^{-3}. Fig. 4 shows the DLTS thermal scans of the electron trap for samples L-119D and Y-015B and Y-015C. The activation energy for this electron trap is E_c-0.31 eV, and the trap density is 6.6×10^{12} cm^{-3} for Y-015B, 6×10^{11} cm^{-3} for Y-015C, and 9.3×10^{10} cm^{-3} for L-119D. The results showed that grown-in defect density is lower in the Ge-doped diode than the Be-diffused diodes. The results further revealed that defect density decreases with increasing "x" in the top p-$Al_xGa_{1-x}As$ window layer indicating that the observed E_c-0.31 eV electron trap is affected by the amount of Al in the p-layer. Fig.5 shows the optical DLTS scans of hole trap (E_v+0.18 eV) for the "Be"-diffused and "Ge"-

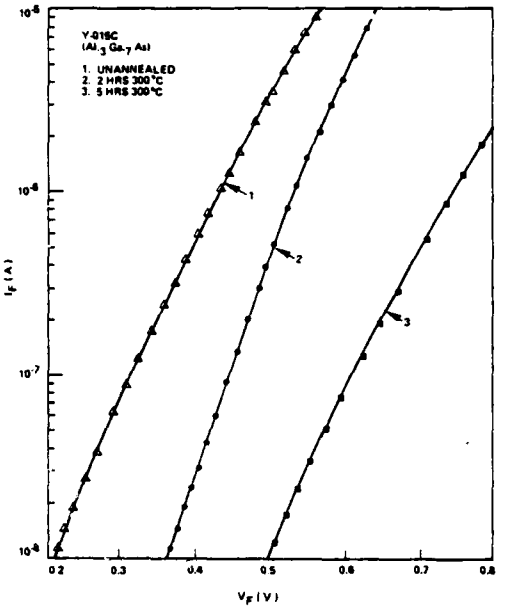

Fig. 3. The forward I-V characteristics curves for diodes Y-015C ($Al_{0.3}Ga_{0.7}As$), before and after 300 °C thermal annealing for 2 and 5 hrs..

doped $Al_{0.3}Ga_{0.7}As$ p-n diodes. The result again showed that the density of this hole trap was lower for the "Ge" doped sample than the "Be"-diffused samples. Possible explanation for the observed results shown in Figs. 4 and 5 is that the "Be" dopant, which was used to form a p-n junction in the $Al_{0.3}Ga_{0.7}As$ LPE layers, is a fast diffusant and can penetrate deeper into the undoped n-$Al_{0.3}Ga_{0.7}As$ LPE layer than the "Ge" impurity. As a result the observed defect density in the undoped n-$Al_{0.3}Ga_{0.7}As$ LPE layer is higher for the "Be" diffused diodes than for the "Ge" doped diodes. Fig. 6 shows the DLTS thermal scans of hole traps for samples Y-015C and L-138D. One hole trap with energy of E_V+0.18 eV was observed in diode Y-015C (in the undoped n-$Al_{0.3}Ga_{0.7}As$ LPE layer) and two hole traps with energy of E_V+0.40 and +0.71 eV were observed for diode L-138D (GaAs LPE layer). The two hole traps (known as "A" and "B" centers) observed in

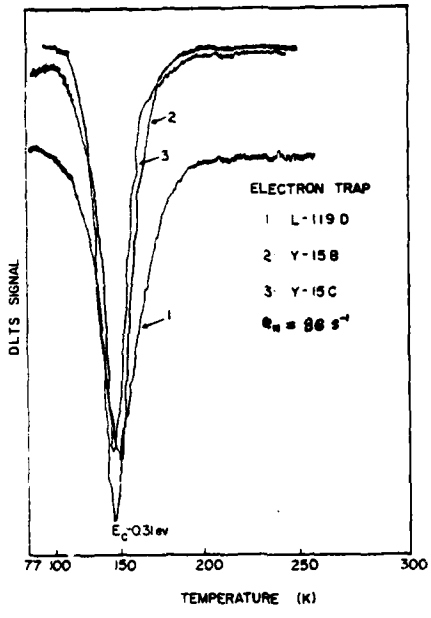

Fig. 4. DLTS thermal scans of the electron trap (E_c-0.31 eV) for the Be-diffused $Al_xGa_{1-x}As$ diodes (Y-015B and Y-015C) and Ge-doped $Al_{0.3}Ga_{0.7}As$ p-n diode (L-119D).

sample L-138D have also been reported in the literature for GaAs [8]. Table 1 summarizes the calculated and measured defect parameters for the undoped n-$Al_{0.3}Ga_{0.7}As$ and n-GaAs LPE layers. Note that calculations of the defect parameters such as trap energy level and density, capture cross section and electron lifetimes from the DLTS and C-V data have been described in our previous publication [9] and will not be elaborated further here.

To investigate the effect of low temperature thermal annealing on the grown-in defects in both the $Al_{0.3}Ga_{0.7}As$ and GaAs LPE layers, we have performed a 300 °C thermal annealing experiment for samples Y-015C and L-138D for 2 and 5 hrs., and the results are shown in Figs. 7 through 9. Fig. 7 shows the DLTS scans of electron trap for three Y-015C

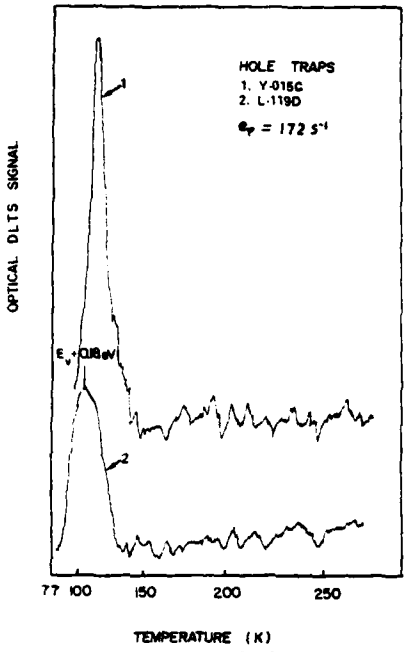

Fig. 5. Optical DLTS scans of the hole trap (E_V+0.18 eV) for diodes Y-015C and L-119D.

samples, one unannealed and two annealed at 2 and 5 hrs., respectively. The results clearly show that defects density decreases with increasing annealing time. Similar results were also obtained for the GaAs LPE layers (L-138D). This is illustrated in Fig. 8 for two electron traps with energy levels of E_C-0.42 and E_C-0.60 eV, and in Fig. 9 for two hole traps with energy levels of E_V+0.40 eV (i.e., "A" center) and E_V+0.71 eV (i.e., "B" center) [8]. Table 2 summarizes the defect parameters deduced from the DLTS data for the unannealed and the annealed samples (Y-015C and L-138D). The results shows that the defect density can be reduced by more than one order of magnitude by a 300 °C anneal for 5 hrs..

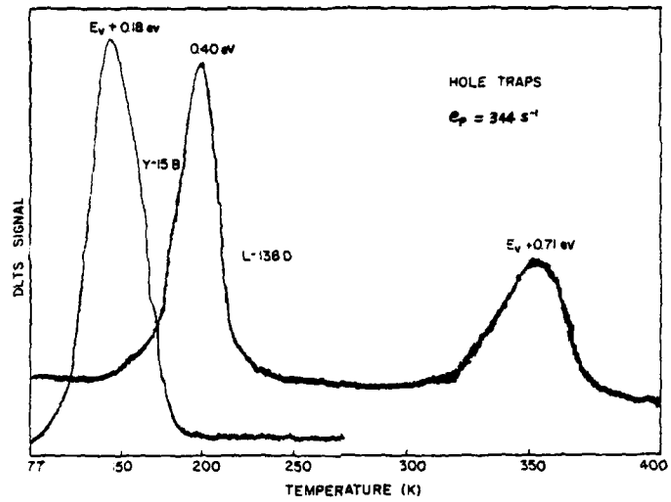

Fig. 6. DLTS thermal scans of the hole traps for diodes Y-015C (E_v+0.18 eV) and L-138D (E_v+0.40 and +0.71 eV).

Conclusions

Characterization of grown-in deep-level defects in the undoped n-$Al_{0.3}Ga_{0.7}As$ and n-GaAs LPE layers using four different junction structures and two different p-dopants has been carried out in this study by employing I-V, C-V, and DLTS measurements. The effect of a 300 °C thermal annealing on the grown-in defects in both $Al_{0.3}Ga_{0.7}As$ and GaAs LPE layers have also been studied. For the undoped $Al_{0.3}Ga_{0.7}$-As LPE layers, one electron trap with energy of E_c-0.31 eV and one hole trap with energy of E_v+0.18 eV were observed in both the "Be" diffused and "Ge" doped $Al_{0.3}Ga_{0.7}As$ samples. It was also observed that by increasing the "Al" contents in the p-$Al_xGa_{1-x}As$ window layer will result in the decrease of the trap density of E_c-0.31 eV level in the undoped $Al_{0.3}$-$Ga_{0.7}As$ LPE layer, the reason for this reduction is not clear and requires further study. As for the GaAs LPE layers, we have observed two electron traps with energy of E_c-0.42 eV (EL1) and E_c-0.60 eV (EL3) and two hole traps with energy

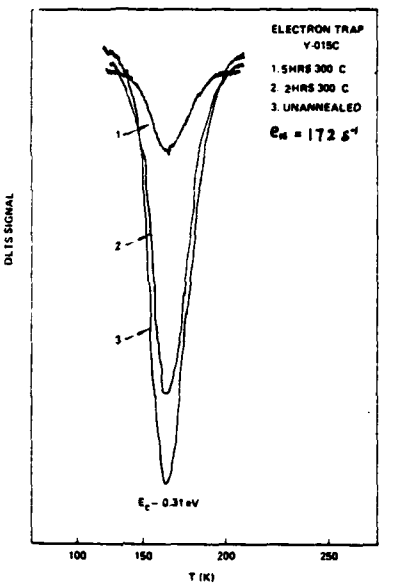

Fig. 7. DLTS thermal scans of the electron trap (E_c-0.31 eV) for three Y-015C diodes, unannealed and annealed at 300 °C for 2 and 5 hrs., respectively.

of E_V+0.40 eV (A) and E_V+0.71 eV (B). The two electron traps observed in our LPE samples have not been observed previously for the GaAs LPE materials but have been observed in the V.P.E. materials [10]. The reason for this may be due to the fact that the density of these two electron traps is very small in the LPE samples (less than 10^{11} cm^{-3}), and can only be detected in a DLTS system operating at a frequency greater than 20 MHz with a sensitivity better than 10^{-4} (i.e., N_{TT}/N_D). From the thermal annealing experiment, it is found that a 300 °C thermal annealing for a few hours can effectively reduce the density of the grown-in defects in both $Al_{0.3}Ga_{0.7}As$ and GaAs LPE layers.

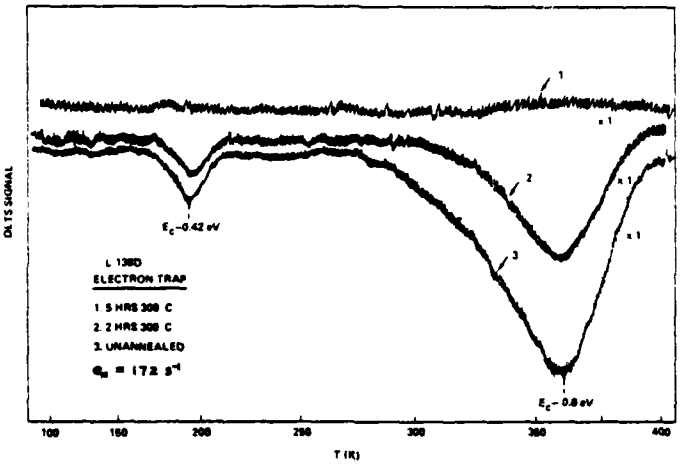

Fig. 8. DLTS thermal scans of the electron traps (E_C-0.42 and -0.60 eV) for three L-138D diodes, unannealed and annealed at 300 °C for 2 and 5 hrs.

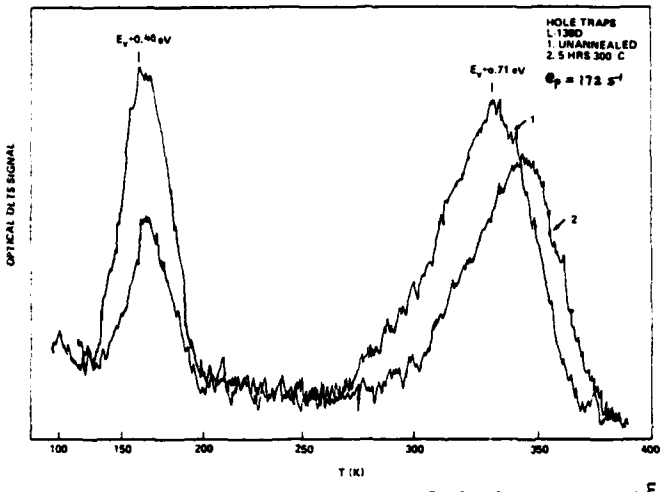

Fig. 9. Optical DLTS thermal scans of the hole traps (E_v+0.40 and +0.71 eV) for two L-138D diodes, annealed at 300 °C for 2 and 5 hrs..

Acknowledgement

The authors (Li and Lin) would like to thank Dr. D. W. Schoenfeld for sample preparation and technical assistance throughout this study. They would also like to acknowledge Dr. W. P. Rahilly for his interests and support in this work.

Table 1. Measured and calculated Defect parameters in n-$Al_{0.3}Ga_{0.7}As$ and n-GaAs LPE layers.

Sample No.	Trap Density (cm^{-3})		Energy level (eV)		Capture Cross Section		Carrier Lifetime		Physical Origin	
	electron	hole	Electron	Hole	σ_n (cm^2)	σ_p	τ_n(μs)	τ_p	Electron	Hole
Y-015B (Be)	6.6×10^{12}	6×10^{12}	E_c-0.31	E_v+0.18	3.27×10^{-13}	-	0.015	-	-	-
Y-015C (Be)	6.0×10^{11}	-	E_c-0.31	-	4.23×10^{-13}	-	0.13	-	-	-
L-119D (Ge)	9.3×10^{10}	-	E_c-0.31	-	4.49×10^{-13}	-	0.79	-	-	-
L-138D	7.1×10^{10}	5.5×10^{10}	E_c-0.42	E_v+0.40	1.29×10^{-12}	-	0.35	-	-	"A"
	1.7×10^{10}	4.1×10^{11}	E_c-0.60	E_v+0.71	1.25×10^{-12}	-	0.23	-	-	"B"

+ $\tau_n = 1/N_{TT}\sigma_n\langle v_n\rangle$; $\langle v_n\rangle = (3kT/m^*)^{1/2}$.

Table 2. Defect parameters for the unannealed and the annealed $Al_{0.3}Ga_{0.7}As$ and GaAs LPE layers.

Diode #	Annealing condition	Electron Traps		Hole Traps		$N_D^*(cm^{-3})$
		E_c-E_T (eV)	$N_{TT}^*(cm^{-3})$	E_v+E_T (eV)	$N_{TT}^*(cm^{-3})$	
Y-015C	unannealed	0.31	6.0×10^{11}	0.18	$<10^{10}$	2.6×10^{16}
Y-015C	300°C, 2 hrs.	0.31	4.4×10^{11}	0.18	"	5.7×10^{16}
Y-015C	300°C, 5 hrs.	0.31	3.6×10^{11}	0.18	"	3.5×10^{16}
L-138D	unannealed	0.42	7.1×10^{10}	0.40	5.5×10^{10}	2.8×10^{15}
		0.60	1.7×10^{11}	0.71	4.1×10^{11}	3.6×10^{15}
L-138D	300°C, 2 hrs.	0.42	1.2×10^{10}	0.40	2.7×10^{10}	2.1×10^{15}
		0.60	4.7×10^{10}	0.71	2.4×10^{10}	2.4×10^{15}
L-138D	300°C, 5 hrs.	0.42	1.0×10^{9}	0.40	1.3×10^{10}	2.5×10^{15}
		0.60	6.6×10^{9}	0.71	1.5×10^{10}	2.4×10^{15}

*N_{TT} is the trap density, and N_D is the carrier density in the undoped n-$Al_{0.3}Ga_{0.7}As$ and n-GaAs LPE layers. N_D was deduced from C-V data and N_{TT} is from DLTS data [9].

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*Research supported in part by the Air Force Wright Aeronautical Laboratories, Aeropropulsion Lab., Wright Patterson Air Force Base, Ohio, subcontract through SCEEE, contract F33615-81-C-2011, task-4, and in part by AFOSR grant no. 81-0187.

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